

High-Speed A/D Converter Designs: Layout and Interfacing Pitfalls ADC-AN-1

By Bob Leonard

A/D converters provide the speed, precision, and resolution needed for today's control systems. Here are some design tips to help you get the most for your money and time.

Understanding the fundamentals of layout in a precision, high-speed, analog-to-digital (A/D) converter is just as important, and sometimes as difficult, as knowing how to design the interface circuitry. Most data sheets will state certain precepts of layout or interface circuitry, but quite often the reasons behind the precepts aren't included. As a result, proper design procedures often aren't followed, and the device is blamed for not living up to its data sheet specifications. The following article outlines design practices to help you avoid A/D layout and interfacing pitfalls that can cost you time and money. The two A/D architectures discussed include successive approximation and two-pass or subranging A/Ds. A third type, the dual-slope A/D, is also quite popular. However, it is better suited for slow-speed applications and thus will not be discussed here.

Grounding

Accurate converter systems begin with good ground management. System ground configurations will vary depending on the size of the overall system, the different magnitudes and locations of the system's analog and digital ground currents, and whether the converter's analog and digital grounds are connected together internally.

For many system designs, optimum performance is achieved when the analog and digital grounds are tied together at the ground plane beneath the converter (Figure 1), and brought back separately to the analog and digital power supplies. An analog signal voltage only has the integrity of its analog ground. When the analog and digital grounds are connected at the power supplies, problems arise; noisy digital ground currents flow through and contaminate the analog ground (Figure 1).

In addition to the noise created, the amplitudes of these currents multiplied by the impedance of the ground, could enter into the millivolt region, causing decreased A/D accuracy. When system requirements mandate the use of a common return to the power supplies for both analog and digital grounds, the converter should be located close to the power supplies. Also, to further minimize impedance-related problems, as large a conductor as possible should be used between the converter and the power supplies.

The extent to which accuracy is threatened by the noise sources just noted is shown by the following example: For a 12 bit converter on a 10 V full scale range, 1/2 LSB (least significant bit) of accuracy is equivalent to 1.22 millivolts; therefore, if a 7 millivolt difference in ground throughout a system exists, a few LSBs of A/Ds accuracy error will result.

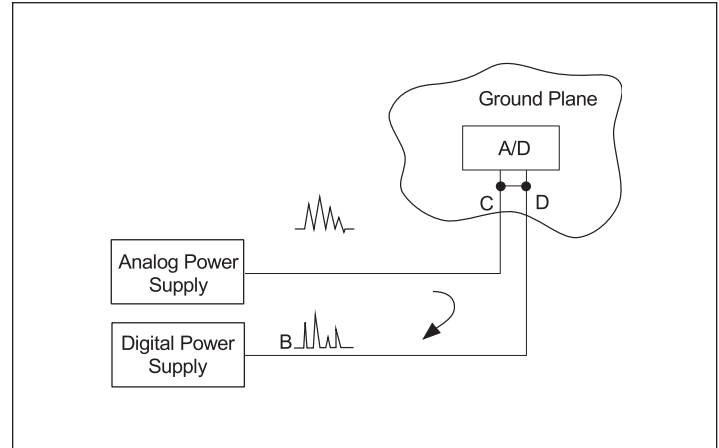


Figure 1. The ideal ground layout joins the analog and digital grounds at the ground plane beneath the converter (pts C & D), not at the power supply (pts A & B), and runs independent grounds to both supplies (A-C & B-D). One non-ideal ground layout joins grounds A & B with only one ground return (A-C) to the A/D, thus contaminating the analog ground return. The classic ground loop (red) combines A & B, runs two returns to C & D, and also combines C & D.

Ground loops occur when analog and digital grounds are tied together at more than one location. For instance, a ground loop might develop if the A/D's analog and digital grounds were connected inside the A/D and also connected by the designer at the power supplies (Figure 1). Noisy digital ground currents would then contaminate the analog ground.

System designs that use more than one converter can result in an unwanted situation – having more than one location in which analog and digital grounds come together. Here, the impedance between converters should be minimized by the use of a large ground plane.

For small systems, separate analog and digital ground return paths (busses) can then be run back from the ground plane to the separated analog and digital power supplies. A large system, however, may have other devices that produce large digital currents and create noise. A/Ds should be located away from these noise sources, to prevent the noise from being introduced into the ground plane beneath the converter. When the distance between the A/D's ground plane and power supplies needs to be long, large digital currents from other circuitry within the system should be returned close to the digital power supply. If this doesn't provide the desired performance, a separate analog return for the converter may be required. This can be done by using local, isolated power supplies (Figure 2).

Decoupling Capacitors

Decoupling capacitors on power supplies are essential to prevent noise spikes and oscillations from degrading converter performance. Noise spikes from digital switching, or the use of switching power supplies, can create problems. Power supply rejection of converter products appears excellent at first glance. For example, the power supply rejection specification of the ADC-500 (DATEL's 12-bit, 500 ns hybrid) gives a 0.01% change in full scale range (FSR) for every

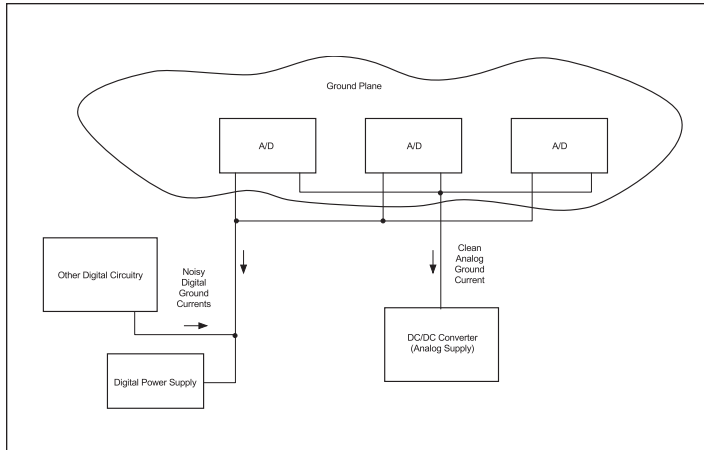


Figure 2. Impedance among converters can be minimized by the use of a large ground plane. A local, isolated analog power supply may be needed to clean up noise.

1% change in the power supply voltage (0.01% FSR/ % Vs). Linear power supplies designed for converter products keep the percentage change less than 0.1% for variations in load. Thus the effect from a maximum change permissible in the power supply would be less than 1/10 of an LSB of the ADC-500. These specifications are at dc, however, and assume clean power supplies. A look at the power supply rejection versus frequency of some amplifiers inside the converters tells the real story. The 100 dB (16 bits of accuracy) power supply rejection at dc quickly degrades to -40 dB (6 bits of accuracy) at a frequency of 10 kHz.

Power lead inductance, combined with stray capacitance on high speed converter devices, can cause oscillations on the supply lines, affecting internal converter components. Obviously, these must be avoided or accuracy will suffer. Bypassing the power supplies directly at the A/D's pins with high frequency decoupling capacitors (0.01 μF ceramic) may still find the circuit ringing. The stray power lead inductance and the capacitance will represent an LC tank circuit whose response for a current step would be oscillation. Paralleling the high frequency decoupling capacitors with low frequency decoupling capacitors (1 μF to 10 μF tantalum) lowers the resonant frequency of the tank circuit (Figure 3). Should the Q of the circuit still not be low enough, the addition of a low value resistor (1 ohm) in series with either of the bypass capacitors will assure fast settling step responses.

Input Drive Requirements of A/Ds

Careful attention must be paid to the input drive requirements of high-speed A/Ds to assure that they'll meet their accuracy requirements. This is especially true for successive approximation types.

The heart of the successive approximation A/D is the internal digital-to-analog converter (D/A) (Figure 4). The D/A's bits, from MSB (most significant bit) to LSB, are successively turned on or off by the successive approximation register (SAR). Upon receiving an initial or an updated code, the D/A must then settle at the comparator input to the accuracy of the device within a time frame controlled by the system clock (e.g. about 150 ns for the 2 μs conversion time of DATEL's 12-bit hybrid ADC-817).

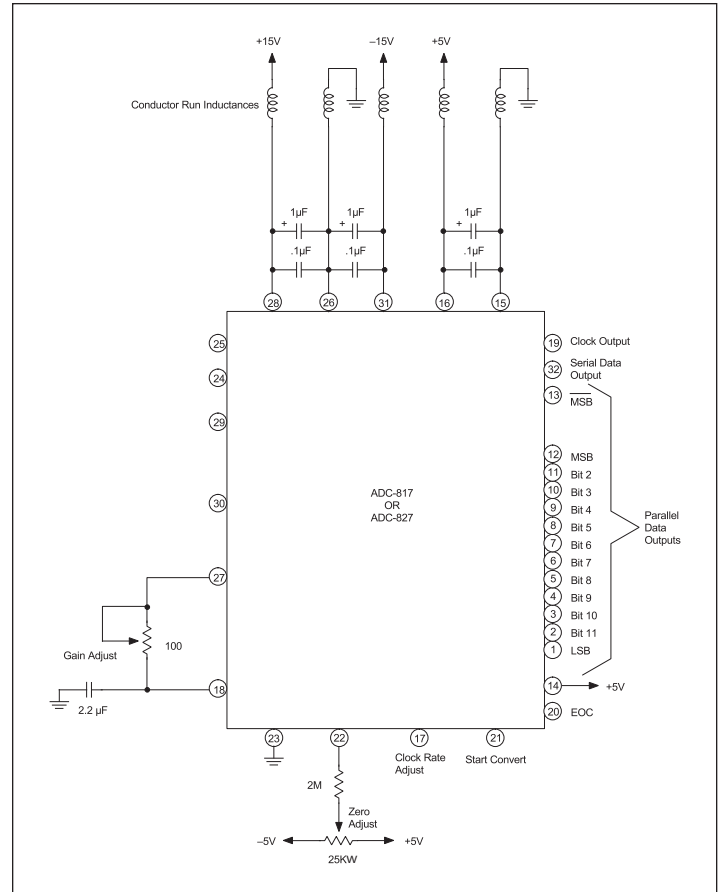


Figure 3. The use of decoupling capacitors assures fast settling step response on the power supplies.

When the comparator receives a strobe from the system clock, the comparator decides whether the analog input is greater or less than the internal DAC output. Each time the DAC is updated to a new value by the SAR, a current pulse is created by the DAC, which is reflected back to the A/D's analog input. The driving source will need to sink or source a proportional current to that which occurs from the DAC undergoing code changes. Failure to provide this current sinking or sourcing before the next comparator strobe will create errors because voltage drops appear across the driving sources output impedance.

In the ADC-817, the current pulse (which results from the internal D/A's code changes) flows through the internal inductance of the conductor runs and bond wires of the hybrid converter. This same current pulse then flows through the user's connections to his driving source. Short leads from the successive approximation A/D are imperative to minimize the resulting inductance of this connection. The D/A current step into the inductance causes ringing – which the driving source must be capable of settling to within the accuracy of the A/D at the signal bandwidth of interest (Figure 5). This settling has to occur before the next comparator strobe (e.g. 150 ns for the ADC-817). This requires the input source amplifier, whether a sample-hold or buffer amplifier, to settle within 150 ns (12 bits).

Thus, it's not enough only to assure that the analog input has settled to the appropriate accuracy before beginning an A/D conversion. The drive source

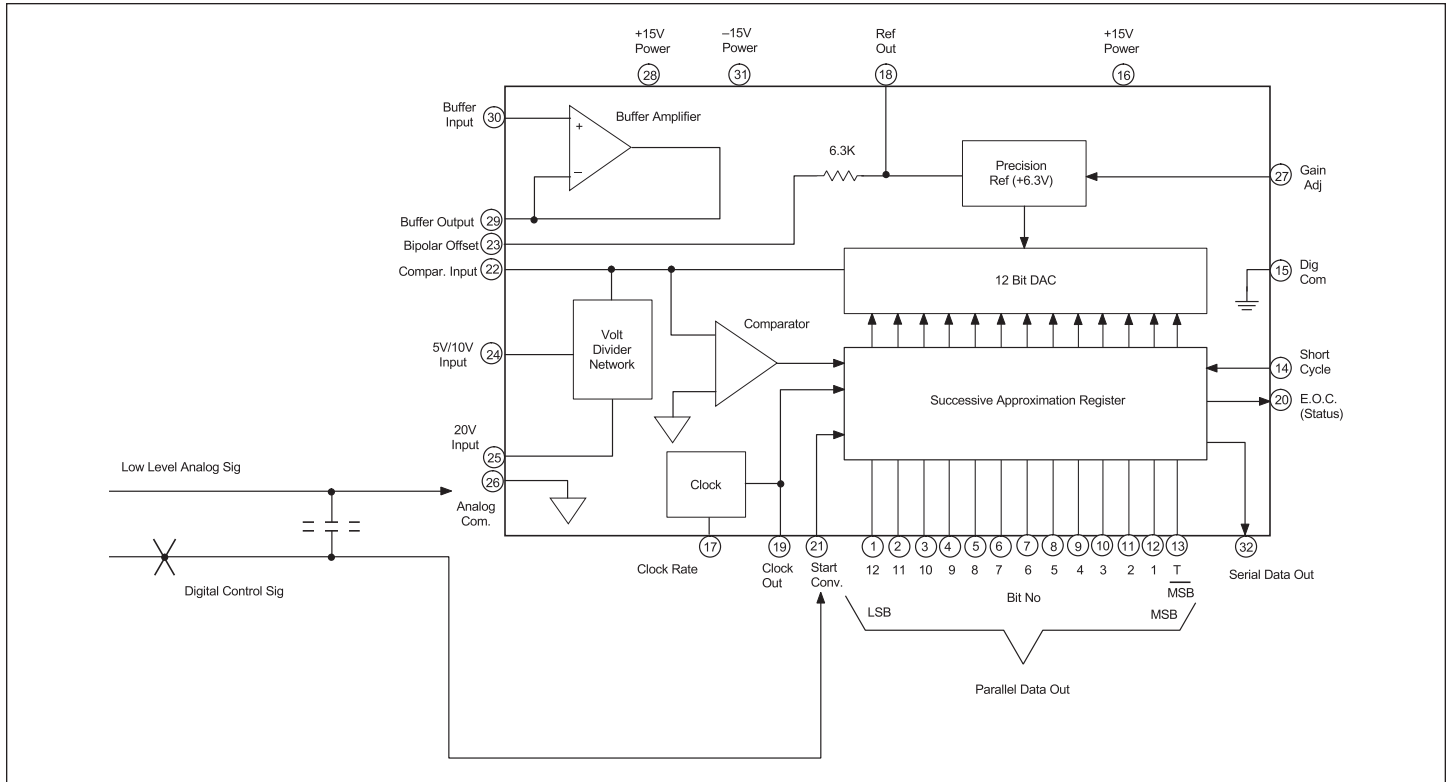


Figure 4. The successive approximation A/D (ADC-817 shown) should have digital control signals routed away from sensitive analog inputs.

must be able to handle the current pulses from the internal D/A and subsequent ringing. Monolithic buffer amplifiers or sample-holds for successive approximation A/Ds may not meet these requirements even for dc inputs. Hybrid driving sources may be required to meet the settling time requirements for the frequencies of interest.

Two-pass or subranging A/Ds have less stringent requirements than successive approximation types. The ADC-500, for example, has its analog input first digitized by a 7-bit flash converter to determine the seven most significant bits. A feedback D/A with 13 bits of linearity subtracts this 7-bit result from the analog input, producing a residual voltage. This residual voltage is amplified and converted by a second pass of the flash converter. This result, along with the first pass, goes to an adder to determine the full 12-bits of the A/D (Figure 6). There are no current pulses from each D/A bit because the D/A feedback occurs in one instance and goes to internal amplifiers of the A/D rather than the analog input. The choice of a buffer amplifier, or sample-hold for a two-pass device, can thus be focused only upon signal bandwidth considerations.

Separation of Analog and Digital Signals

Precision A/Ds handle very low level signals – into the millivolt and microvolt range. Contamination of these analog signals can occur from charge injection caused by changing digital logic levels leaking through stray capacitance (Figure 4). Extreme care should be taken to route digital lines away from sensitive analog inputs, references, offset, and gain adjustment input pins. Shielding sensitive analog signals and the use of low impedance paths (ground planes)

around sensitive analog input pins may be required to assure trouble-free operation.

Avoiding Dynamic Linearity Errors

The successive approximation A/D architecture has critical time constraints to accomplish internal functions to meet its accuracy specification. Inside, when the successive approximation register turns a D/A bit on, the D/A is allotted a certain time frame to settle at the comparator input. Upon receipt of the system clock strobe, the comparator decides what the equivalent logic level will be set

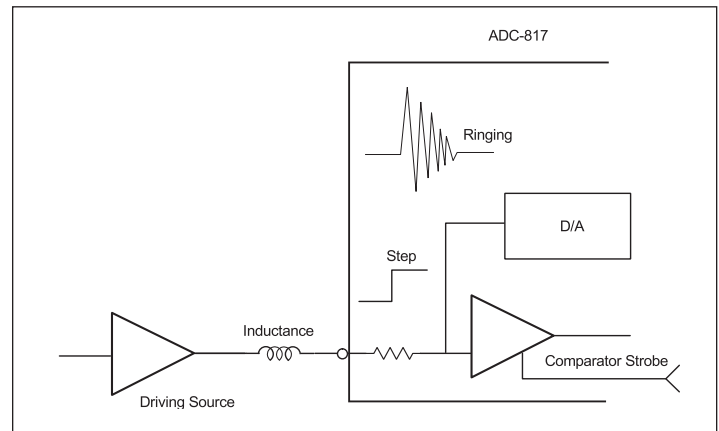


Figure 5. Inductance of external and internal conductor runs causes ringing which the driving source must settle before the clock strobes the comparator.

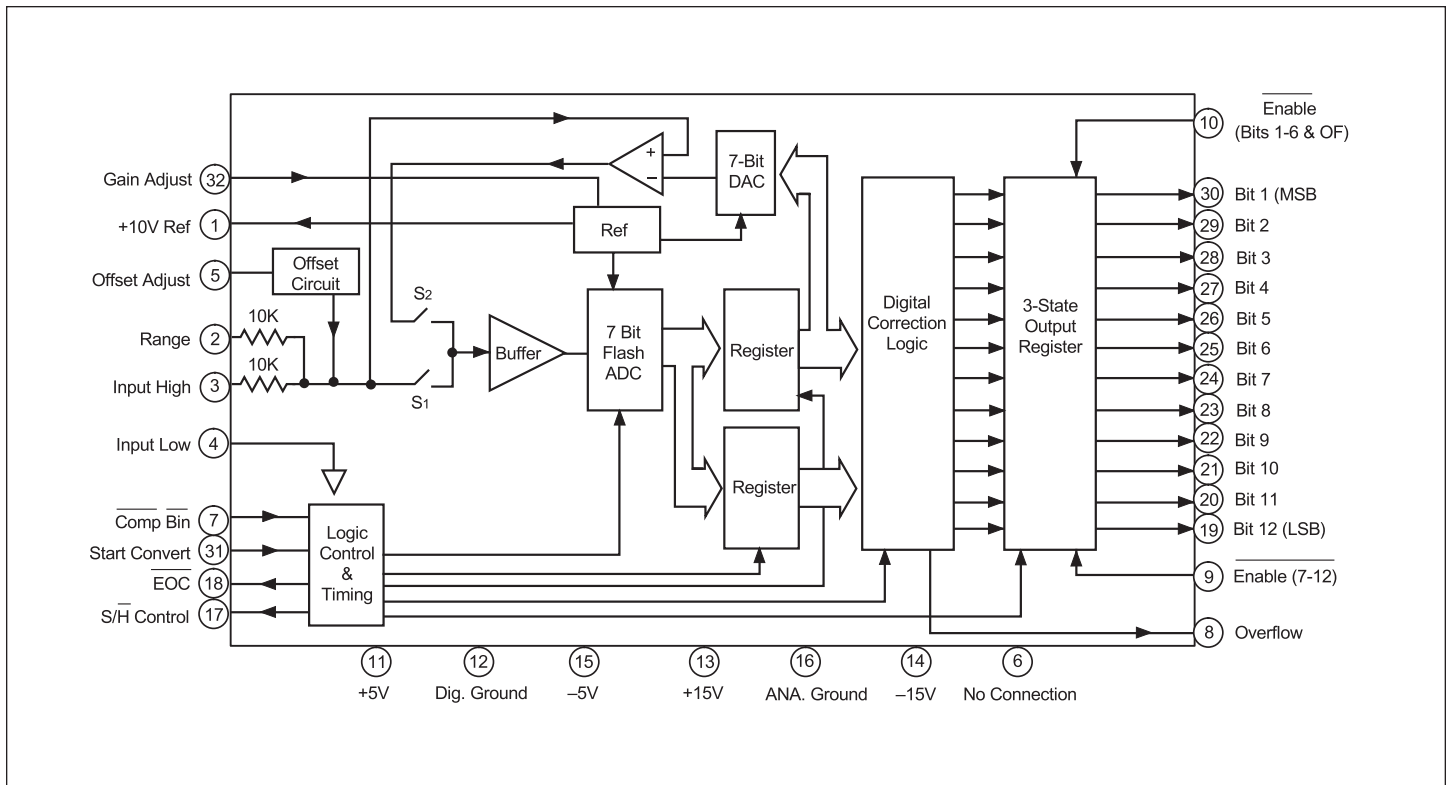


Figure 6. Block diagram of a two-pass or subranging A/D (DATEL ADC-500).

for the A/D bit. A/D transfer errors, which result because of the D/A's unsettled state to the full accuracy before the comparator makes its decision, often are referred to as dynamic linearity errors.

Many high speed successive approximation A/D converters do not have output latches for the parallel output data. Therefore, these output latches are required external to the converter. The unbuffered outputs of the A/D's SAR are also the internal D/A's digital inputs. When the D/A bit is turned on, there is an exponential rise time as the bit goes to a high logic level (Figure 7). Stray capacitance from long leads to output latches can prevent the D/A from turning

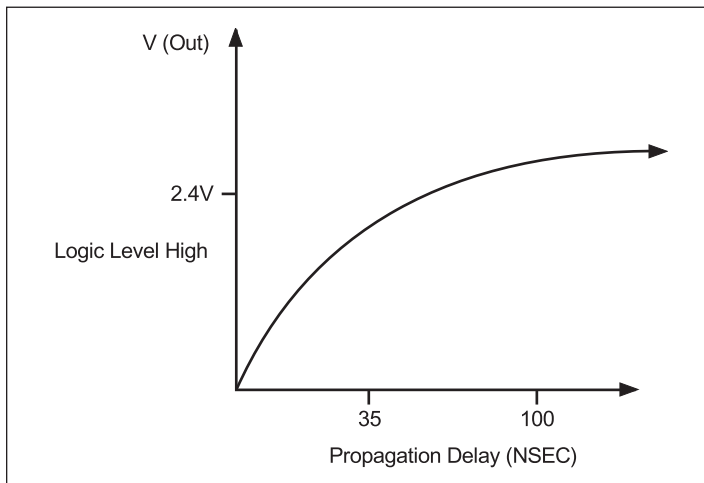


Figure 7. Stray capacitance increases rise time for a digital logic high level.

on as quickly as is needed, thus reducing the D/A settling time. Upon receiving the clock strobe, the comparator will make a decision – whether or not the D/A has settled to the required accuracy. Therefore, the distance from the parallel output data to the output latches should be kept to less than one inch to prevent dynamic linearity errors (Figure 8).

The comparator input of the successive approximation A/D is normally brought to an external pin on the A/D. This allows offsetting for bipolar full scale ranges and adjustment of initial offset errors through the use of external trim pots. Note that the comparator input is also the internal D/A's output. Capacitance appearing on the D/A output can also prevent the D/A from settling to full accuracy within its allotted time frame. Stray capacitance must be minimized on this pin to assure proper settling. The offset adjustments wiper resistor should be located extremely close to the A/D to avoid stray capacitance on the comparator input.

Unipolar configurations do not require the bipolar offset pin to be tied to the comparator input. However, the nature of bipolar operation requires offsetting the comparator input by tying the bipolar offset pin to the comparator input. Most A/Ds locate the comparator input and bipolar offset pins next to each other so this connection can be kept very short. Also, some A/Ds are dedicated for either unipolar or bipolar configurations; therefore, they inherently prevent additional capacitance from being added when they are being used in a bipolar configuration.

Avoid Long Conductor Runs

Although the bipolar offset pin is located next to the comparator input (Figure 4), a short connection is not always possible. When wiring to external cards,

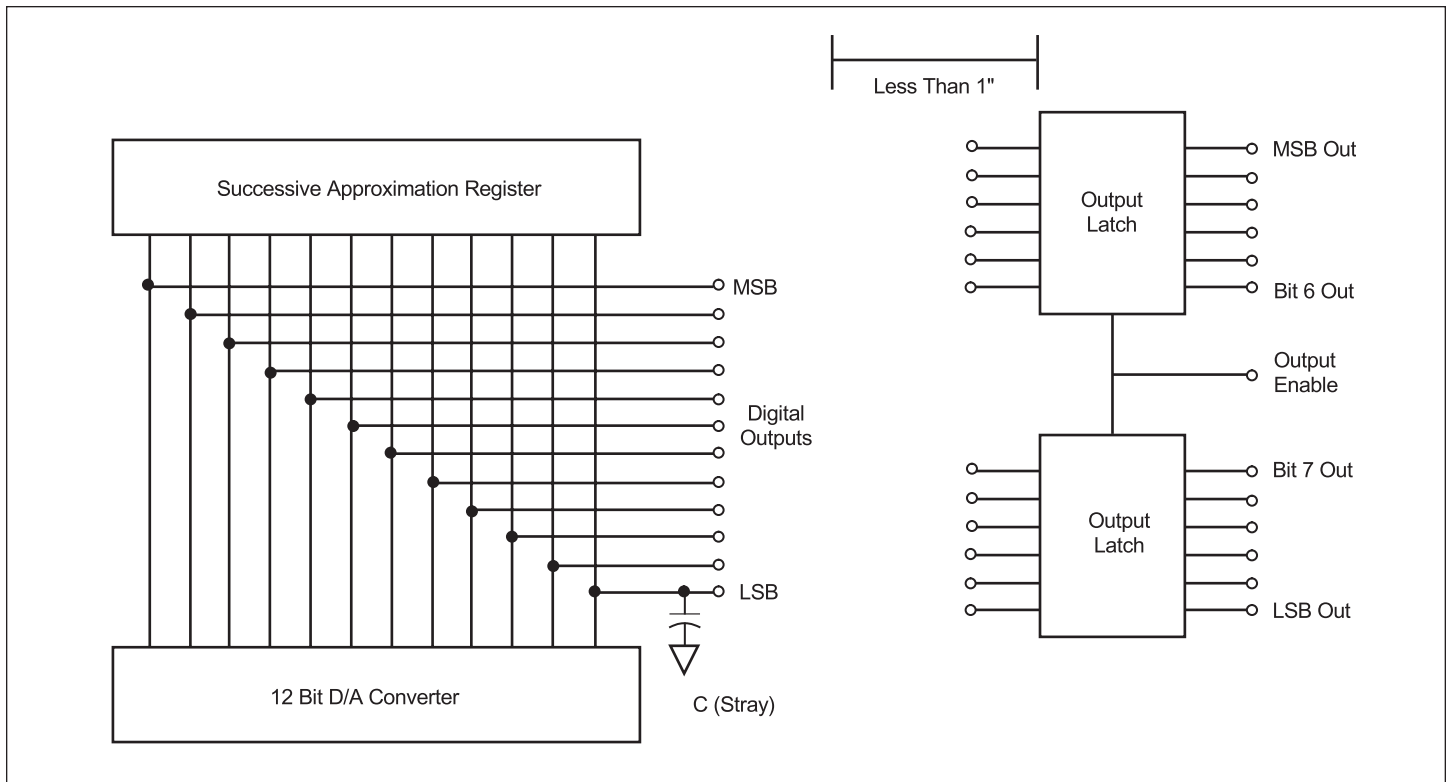


Figure 8. Parallel outputs of successive approximation A/Ds are the internal D/A's inputs. Keep these signal paths less than one inch in length

use only low capacitance switches, short leads, and a large ground plane. System layouts, which enable the end-user to pin-strap the A/D for unipolar or bipolar operation, often involve long conductor runs for ease of mode selection. These, however, make the comparator input susceptible to capacitance and

noise pickup. Two-pass architectures do not incur these dynamic linearity failures because of the nature of their operation.

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