Modifying Start Convert Pulses Using Commercially Available Devices
ADC-AN-07

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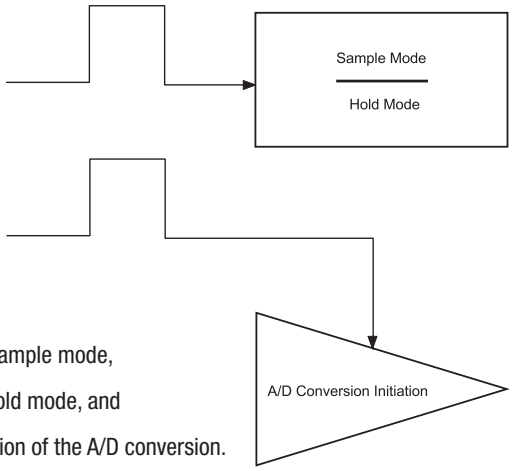
This application note provides DATEL's sampling analog-to-digital (A/D) converter customers with two methods of adjusting the start convert pulse width.

The start convert input pulse is very critical to the operation of a sampling analog-to-digital (A/D) converter because it directly controls some of the internal timing of the device. To assure proper operation, a thorough study and clear understanding of the device's characteristics is essential.

Before discussing how to adjust the pulse width, let's explore just how critical the accuracy of a trigger pulse is to the operation of a sampling A/D converter. In most cases, any variation from the specified pulse width will lead to malfunctioning of the device.

Historically, design engineers had to carefully control the timing of three different functions:



1 – The sample mode,

2 – the hold mode, and

3 – initiation of the A/D conversion.

This often meant that the user had to generate at least two pulses.

New Technology Provides an Answer.

The last few years have seen a growing popularity of sampling A/D's. Their availability is largely a response to the demand for higher conversion speeds and resolutions.

These devices incorporate internal gate array and logic circuitry, providing the necessary timing sequences which are triggered off a single external start convert pulse. Users, in most cases, only have to provide one pulse to control all operations.

As an example, DATEL's ADS-117 specifies a pulse width (t w) of 50 nanoseconds (30 nsec. minimum, 60 nsec. maximum) for proper operation at a sampling rate of 2 MHz. A timing diagram of the ideal situation would look like the one shown in Figure 1.

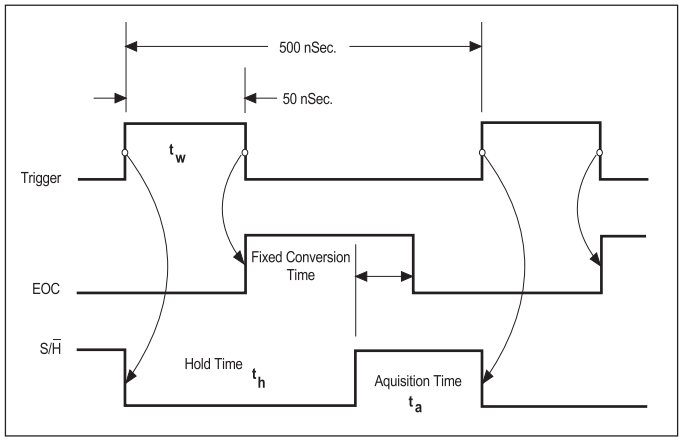


Figure 1. Accurate Trigger Pulse

Effects of Changing the Pulse Width

With too short a pulse width...

If the pulse width of the trigger pulse is *shorter* than the recommended 30 nanoseconds, minimum, (t_W = 20 ns), the design engineer would violate the *hold mode settling time.* This is the time from the hold command transition until the output of the sample-hold settles to within a specified accuracy.

th1 < th (hold mode settling time required)

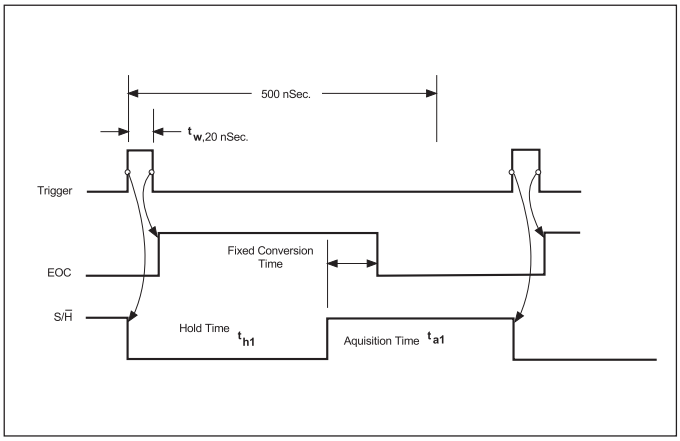


Figure 1a. Effects of a Short Trigger Pulse

With too long a pulse width...

Operating at the maximum speed with a *longer* than recommended trigger pulse, (t_W = 100 ns), would violate the device's acquisition time specification, in addition to creating a droop concern.

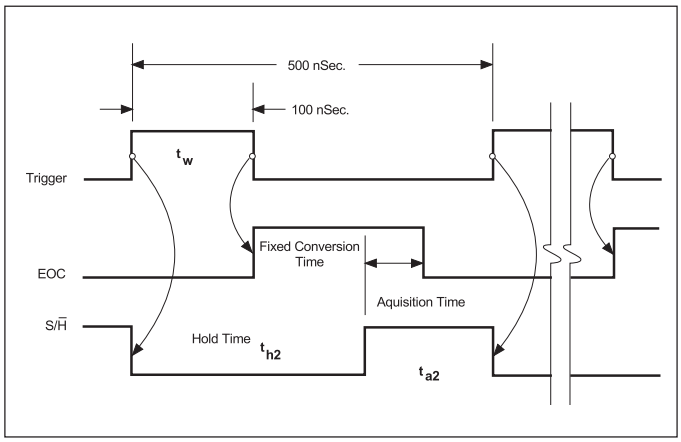


Figure 1b. Effects of a Long Trigger Pulse

In this example, the acquisition time (t_{a2}) is smaller than the specified time (t_a) needed for the hold capacitor of the sample/ hold to charge to a full scale voltage and then remain within a specified accuracy around the final value.

The following discussion explains only two of the many ways to adjust the pulse width of a digital signal.

Both circuit descriptions that follow assume that the period of the applied external clock (t_1) is greater than the pulse-width being created (t_2), as shown in Figure 2. In the example using a D-type flip-flop, t1 must be at least twice as large as t_2.

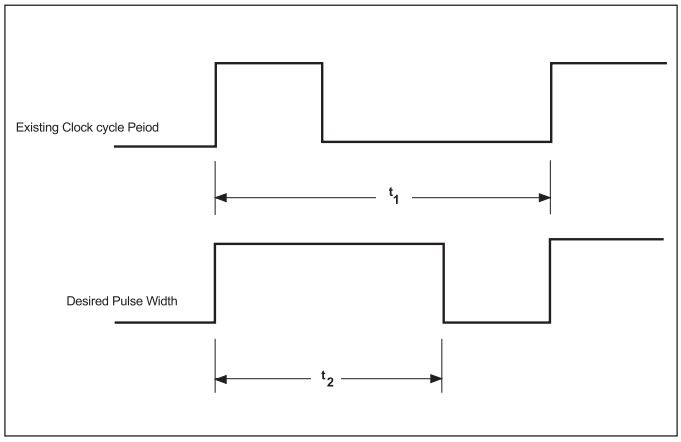


Figure 2. Pulse Width Relationships

Creating an Accurate Pulse

Option A – Using a D-Type Flip-Flop

As an intermediate device between the trigger pulse and the start convert input of the A/D converter, a D-type flip-flop with an external resistor and capacitor lets the design engineer vary the pulse width as required.

The flip-flop recommended is a D-type positive-edge-triggered Series 54ACT74 sold by National Semiconductor, Motorola, RCA, and other vendors. These devices have independent DATA, $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs, with Q and Q outputs. The logic level resent at the data input is transferred to the output during the positive-going transition of the clock pulse (CP). $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are active low inputs.

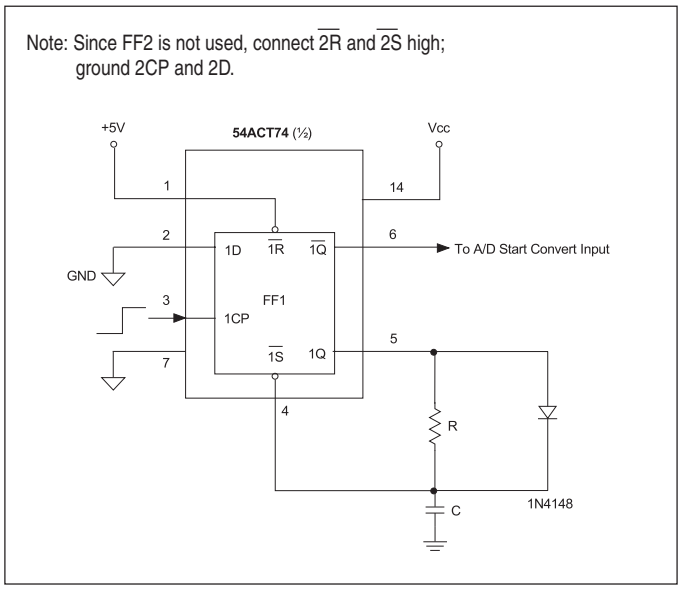


Figure 3. Connections for 54ACT74 Dual Flip-Flop

TRUTH TABLE

Inputs				Outputs	
$\overline{Set}$	$\overline{Reset}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High level (steady state)

L = Low level (steady state)

X = Don't care

⌐ = Transition from low to high level.

Q0 = the level of Q before indicated input conditions.

*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Circuit Description

Adding an external resistor and capacitor to the flip-flop, as shown in Figure 3, creates a delay at the SET input. This time delay corresponds to the pulse width (t_2) of Q which is directly proportional to the resistor and capacitor values used ($t_2 \approx R \times C$).

Preconditions: D is tied low, $\overline{R}$ is tied high, $\overline{S}$ is high initially. See Figure 3.

At the rising edge of the clock pulse, $\overline{Q}$ goes high while Q goes low. This change forces $\overline{S}$ to go low after the time delay (t_2) caused by the resistor/ capacitor circuit connected between Q and $\overline{S}$.

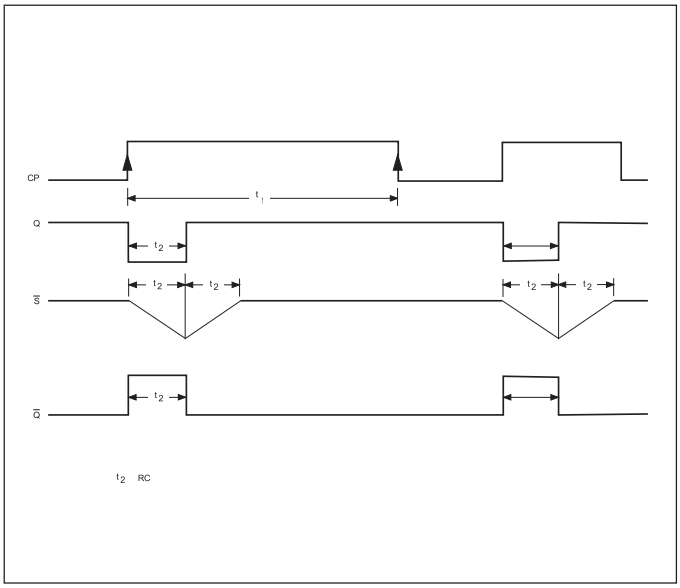


Figure 4. Input/Output Timing Relationships

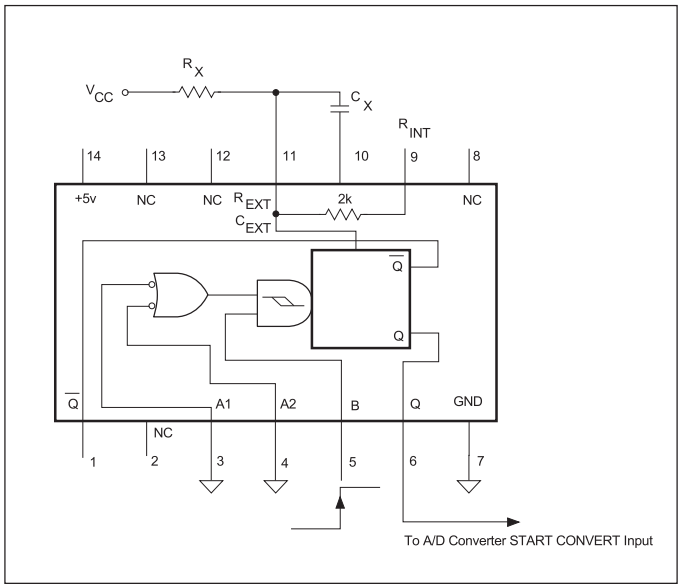


Figure 5. Typical Series '121' Connections for Pulse Generation

Now $\overline{SET}$ is low and $\overline{RESET}$ is high, so automatically $\overline{Q}$ goes low and Q goes high. This drives $\overline{S}$ back to a high state after a similar time delay, completing the cycle.

This explains why ti should be greater than 2 x t_2 . If $\overline{S}$ stays low, the flip-flop will not respond to a retriggered CP input. Adding a diode across R, also shown in Figure 3, speeds up the transition of $\overline{S}$ from low to high, allowing a quicker retriggering of the clock input pulse.

The design engineer should test different values of R and C to get the exact pulse width required. For limitations and operating conditions of the 54ACT74, refer to the vendor's data sheet.

Creating an Accurate Pulse

Option B – Using a Multivibrator

Another way of obtaining the required pulse width is by using a multivibrator. The multivibrator suggested is a Series '121' supplied by Motorola, National Semiconductor, Texas Instruments, and other vendors. A simple RC time constant determines the output pulse width. The RC circuit may consist of external components or an external capacitor and an and an internal 2K ohm resistor. Figure 5 shows a typical connection scheme; for operating conditions of the '121,' refer to the vendor's data sheet.

FUNCTION TABLE

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	H	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

The multivibrator should be set up as follows:

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	↑	⊓	⊔

Circuit Description

The basic output pulse width is determined by using an external capacitor (Cx) in conjunction with a resistor, as shown in Figure 5. The internal 2 kΩ resistor may be used instead of an external resistor (R) by connecting RINT (pin 9) to Vcc (pin 14). The pulse width can vary from 30 nanoseconds to 28 seconds.

1. To determine the pulse width when C_X >1000 pF, refer to Figure 6.
2. For C ³1000 pF, the output pulse width (t) is determined as follows:

$$t_W = K \times R_X \times C_X$$

Where:

R is in kΩ
C_X is in pF
t_W is in nanoseconds
K ≈ 0.7

NOTE: The "K" coefficient is not a constant, but varies as a function of the timing capacitor, C_X. Figure 7 details this characteristic.

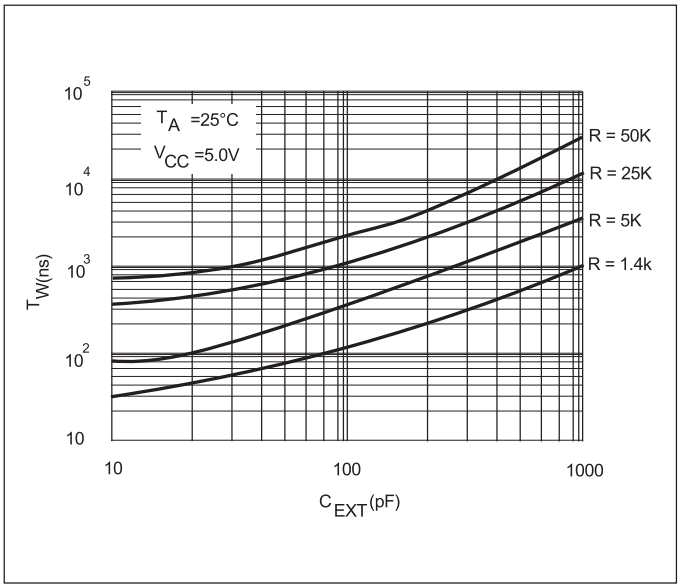


Figure 6. Typical Output Pulse Width vs. External Timing Capacitance

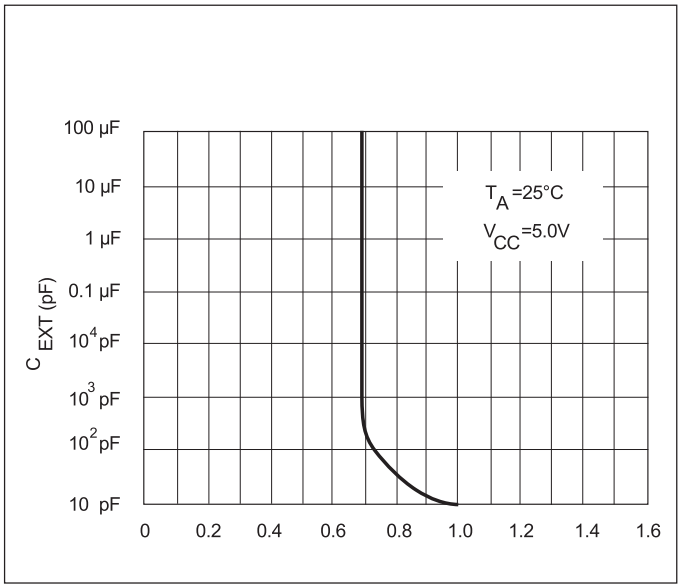


Figure 7. "K" Coefficient