FEATURES
- 8-bit flash A/D converter
- 20MHz sampling rate
- 10MHz full-power bandwidth
- Sample-hold not required
- Low power CMOS
- +5Vdc operation
- 1.2 Micron CMOS
- 8-Bit latched outputs
- Surface-mount version
- No missing codes

PRODUCT OVERVIEW
The ADC-208A utilizes an advanced VLSI 1.2 micron CMOS in providing 20MHz sampling rates at 8-bits. The flexibility of the design architecture and process delivers latch-up free operation without external components and operation over the full military range.

The ADC-208A is mechanically and electrically equivalent to the ADC-208 Series, with the exception of the OVERFLOW (pin 13) and ENABLE (pins 11 and 12) functions. These functions are not offered on the ADC-208A.

INPUT/OUTPUT CONNECTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>FUNCTION</th>
<th>Pin</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>24</td>
<td>BIT 8 (LSB)</td>
</tr>
<tr>
<td>2</td>
<td>CLOCK INPUT</td>
<td>23</td>
<td>BIT 7</td>
</tr>
<tr>
<td>3</td>
<td>REFERENCE</td>
<td>22</td>
<td>BIT 6</td>
</tr>
<tr>
<td>4</td>
<td>ANA/DIG GND (VSS)</td>
<td>21</td>
<td>BIT 5</td>
</tr>
<tr>
<td>5</td>
<td>ANALOG INPUT</td>
<td>20</td>
<td>REF 1/4 FS</td>
</tr>
<tr>
<td>6</td>
<td>REF MIDPOINT</td>
<td>19</td>
<td>VDD</td>
</tr>
<tr>
<td>7</td>
<td>ANALOG INPUT</td>
<td>18</td>
<td>REF 3/4 FS</td>
</tr>
<tr>
<td>8</td>
<td>ANA/DIG GND (VSS)</td>
<td>17</td>
<td>BIT 4</td>
</tr>
<tr>
<td>9</td>
<td>+REFERENCE</td>
<td>16</td>
<td>BIT 3</td>
</tr>
<tr>
<td>10</td>
<td>VDD</td>
<td>15</td>
<td>BIT 2</td>
</tr>
<tr>
<td>11</td>
<td>N.C.</td>
<td>14</td>
<td>BIT 1 (MSB)</td>
</tr>
<tr>
<td>12</td>
<td>N.C.</td>
<td>13</td>
<td>N.C.</td>
</tr>
</tbody>
</table>

Figure 1. ADC-208A Block Diagram
### Functional Specifications

(Typical at +5V power, +25°C, 20MHz clock, +REFERENCE = +5V, –REFERENCE = ground, unless noted)

<table>
<thead>
<tr>
<th>ANALOG INPUT</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-Ended, Non-Isolated Input Range DC - 20MHz</td>
<td>0 – +5.0 Volts</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| ANALOG INPUT Capacitance | (static - Pin 5 to 7) | – 20 – pF |
| Reference Ladder Resistance | – 500 – Ohms |
| Digital Outputs (short circuit protected to ground) | – 0.5 to +VDD Volts |

| REFERENCE Input (Note 5) | –0.5 – +1.0 Volts |

| DIGITAL INPUTS | Logic Levels | Logic **1** | 3.2 – — Volts |
| Logic **0** | — — 0.8 Volts |
| Logic Loading | Logic Loading **1** | — +1 +5 μA |
| Logic Loading **0** | — +1 +5 μA |
| Clock Low Pulse Width | 15 25 — nSec |

| DIGITAL OUTPUTS | Logic Levels | Logic **1** | 2.4 4.5 5.0 Volts |
| Logic **0** | — — 0.4 Volts |
| Logic Loading | Logic Loading **1** | 4 — — mA |
| Logic Loading **0** | 4 — — mA |
| Output Data Valid Delay From Rising Clock Edge | 99% probability | 5 10 15 nSec |
| 100% probability | +25°C | 5 10 25 nSec |
| –55°C to +125°C | — — 40 nSec |
| Data Output Resolution | 8 — — Bits |
| Data Coding | Straight binary |

| PERFORMANCE | Sampling Rate | 15 20 — MSPS |
| Full Power Bandwidth | 10 — — MHz |

| DIFF. LINEARITY @ +25°C | Code Transitions | ±0.5 ±1.0 LSB |
| Center of Codes | ±0.25 — LSB |

| DIFF. LINEARITY OVER TEMP. | Code Transitions | ±0.5 ±1.0 LSB |
| Center of Codes | ±0.25 — LSB |

| INT. LINEARITY @ +25°C (See tech note 4)(ref. adjusted) | End-point | — — ±1/2 LSB |

| ABSOLUTE MAXIMUM RATINGS | LIMITS | UNITS |
| Power Supply Voltage (VDD Pin 1, 10, 19) | –0.5 to +7 Volts |
| Digital Inputs | –0.5 to +5.5 Volts |
| Analog Input | –0.5 to (+VDD +0.5) Volts |
| Reference Inputs | –0.5 to +VDD Volts |
| Digital Outputs (short circuit protected to ground) | –0.5 to +5.5 Volts |
| Lead Temperature (10 sec. max.) | +300 °C |
| Storage Temperature | –65 to +150 °C |

### Best-fit Line

| INT. LINEARITY OVER TEMP. | (ref. adjusted) | ±1/2 ±1 LSB |

### Performance

<table>
<thead>
<tr>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
</tr>
</thead>
</table>

### Best-fit Line

| INT. LINEARITY OVER TEMP. (ref. unadjusted) | End-point | ±2 ±2.6 LSB |
| Best-fit Line | ±1.6 ±1.9 LSB |

### Zero-Scale Offset

| Harmonic Distortion (8MHz second order harm.) | –40 –46 — dB |
| Ref. bandwidth (See tech note 5) | 10 — MHz |
| Power Supply Rejection | ±0.02 ±0.05 %FSR/%Vs |

### No Missing Codes

<table>
<thead>
<tr>
<th>OVER THE OPERATING TEMPERATURE RANGE</th>
</tr>
</thead>
</table>

### Power Requirements

| Power Supply Range (+VDD) | +3.0 +5.0 +5.5 Volts |
| Power Supply Current | +25°C | +45 +65 mA |
| +85°C | +60 +60 mA |
| –60°C | +50 +70 mA |
| +125°C | +40 +60 mA |
| –55°C | +50 +70 mA |
| Power Dissipation | +25°C | 225 325 mW |
| +85°C | 200 300 mW |
| –60°C | 250 350 mW |
| +125°C | 200 300 mW |
| –55°C | 250 350 mW |

### Physical/Environmental

<table>
<thead>
<tr>
<th>OPERATING TEMP. RANGE, CASE:</th>
</tr>
</thead>
</table>

| MC/LC Versions | 0 — +70 °C |
| MC-C/LC-C Versions | 0 — +70 °C |
| ME/LE Versions | –40 — +100 °C |
| ME-C/LE-C Versions | –40 — +100 °C |
| MM/LM/QL Versions | –55 — +125 °C |
| MM-C/LM-C/QL-C Versions | –55 — +125 °C |
| STORAGE TEMP. RANGE | –65 — +150 °C |

### Package Type

| DIP 24-pin ceramic DIP LCC 24-pin ceramic LCC |

### Footnotes:

1. Maximum input impedance is a function of clock frequency.
2. At full-power input.
3. For 10-step, 40 IRE NTSC ramp test.

Footnotes: ➊ Maximum input impedance is a function of clock frequency. ➋ At full-power input. ➌ For 10-step, 40 IRE NTSC ramp test.
TECHNICAL NOTES
1. The Reference ladder is floating with respect to VDD and may be referenced anywhere within the specified limits. AC modulation of the reference voltage may also be utilized; contact DATEL for further information.
2. Clock Pulse Width – To improve performance when input signals may exceed Nyquist bandwidths, the clock duty cycle can be adjusted so that the low portion (sample mode) of the clock pulse is 15nSec wide. Reducing the sampling time period minimizes the amount the input voltage slews and prevents the comparators from saturating.
3. A full-scale input produces all “1” on the data outputs.
4. DATEL uses the conservative definitions when specifying Interval Linearity (end-point) and Differential Linearity (code transition). The specifications using the less conservative definition have also been provided as a comparative specification for products specified this way.
5. The process that is used to fabricate the ADC-208A eliminates the latchup phenomena that has plagued CMOS devices in the past. These converters do not require external protection diodes.
6. Zero Adjustment - Adjusting the voltage at –REFERENCE (pin 3) adjusts the offset or zero of the device. Pin 3 can be tied to GROUND for operation without adjustments.
7. Connect the converter appropriately; a typical connection circuit is shown in Figure 2. Then apply an appropriate clock input. The reference input should be held to ±0.1% accuracy or better. Do not use the +5V power supply as a reference without precision regulation and high-frequency decoupling capacitors.
8. Zero Adjustment - Adjusting the voltage at –REFERENCE (pin 3) adjusts the offset or zero of the device. Pin 3 can be tied to GROUND for operation without adjustments.
9. Full Scale Adjustment - Adjusting the voltage at +REFERENCE (pin 9) adjusts the gain of the device. Pin 9 can be tied directly to a +5V reference for operation without adjustment.
10. Integral Nonlinearity Adjustments - Provision is made for optional adjustment of Integral Nonlinearity through access of the reference’s ¼, ½, and ¾ full scale points. For example, the REF. MIDPOINT (pin 6) can be tied to a precision voltage halfway between +REFERENCE and –REFERENCE. Pins 6, 18 and 20 should be bypassed to GROUND through 0.1μF capacitors for operation without INL adjustments.

Table 1. ADC-208A Output Code

<table>
<thead>
<tr>
<th>ANALOG INPUT</th>
<th>CODE</th>
<th>DATA 1234</th>
<th>DATA 5678</th>
<th>DECIMAL</th>
<th>HEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00V</td>
<td>Zero</td>
<td>0000</td>
<td>0000</td>
<td>0</td>
<td>00</td>
</tr>
<tr>
<td>+0.02V</td>
<td>+1</td>
<td>0000</td>
<td>0001</td>
<td>1</td>
<td>01</td>
</tr>
<tr>
<td>+1.28V</td>
<td>+½</td>
<td>0010</td>
<td>0000</td>
<td>64</td>
<td>40</td>
</tr>
<tr>
<td>+2.54V</td>
<td>+¼ FS-ILSB</td>
<td>0111</td>
<td>1111</td>
<td>127</td>
<td>7F</td>
</tr>
<tr>
<td>+2.58V</td>
<td>+½ FS</td>
<td>1000</td>
<td>0000</td>
<td>128</td>
<td>80</td>
</tr>
<tr>
<td>+2.58V</td>
<td>+½ FS+ILSB</td>
<td>1000</td>
<td>0001</td>
<td>129</td>
<td>81</td>
</tr>
<tr>
<td>+3.84V</td>
<td>+¾ FS</td>
<td>1100</td>
<td>0000</td>
<td>192</td>
<td>C0</td>
</tr>
<tr>
<td>+5.10V</td>
<td>+FS</td>
<td>1111</td>
<td>1111</td>
<td>255</td>
<td>FF</td>
</tr>
</tbody>
</table>

Note: Values shown here are for a +5.12Vdc reference. Scale other references proportionally (+REF=+5.12V, –REF=GND, ¼, ½, and ¾ References FS=No Connection)
MECHANICAL DIMENSIONS

Figure 3. Timing Diagram

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>MODEL</th>
<th>TEMP. RANGE</th>
<th>PACKAGE</th>
<th>ROHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC-208AMC</td>
<td>0°C to +70°C</td>
<td>24-pin DIP</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208AMC-C</td>
<td>0°C to +70°C</td>
<td>24-pin DIP</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208AME</td>
<td>−40°C to +100°C</td>
<td>24-pin DIP</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208AME-C</td>
<td>−40°C to +100°C</td>
<td>24-pin DIP</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208AMM</td>
<td>−55°C to +125°C</td>
<td>24-pin DIP</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208AMM-C</td>
<td>−55°C to +125°C</td>
<td>24-pin DIP</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208AMM-QL</td>
<td>−55°C to +125°C</td>
<td>24-pin DIP</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208AMM-QL-C</td>
<td>−55°C to +125°C</td>
<td>24-pin DIP</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208ALC</td>
<td>0°C to +70°C</td>
<td>24-pin LCC</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208ALC-C</td>
<td>0°C to +70°C</td>
<td>24-pin LCC</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208ALE</td>
<td>−40°C to +100°C</td>
<td>24-pin LCC</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208ALE-C</td>
<td>−40°C to +100°C</td>
<td>24-pin LCC</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208ALM</td>
<td>−55°C to +125°C</td>
<td>24-pin LCC</td>
<td>No</td>
</tr>
<tr>
<td>ADC-208ALM-C</td>
<td>−55°C to +125°C</td>
<td>24-pin LCC</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208ALM-QL</td>
<td>−55°C to +125°C</td>
<td>24-pin LCC</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC-208ALM-QL-C</td>
<td>−55°C to +125°C</td>
<td>24-pin LCC</td>
<td>Yes</td>
</tr>
</tbody>
</table>