DATEL®
INNOVATION and EXCELLENCE

ADCDS-1603

16-Bit, 2.3 Megapixels/Second CCD Image Converter

FEATURES

- 2.3 MPPS
- Internal 16-bit resolution A/D
- Internal correlated doubler sampler (CDS)
- Resistor programmable gain adjustment from 0dB to 15.5dB
- 1.7 LSB RMS Noise @ 2.3MPPS
- Low-Profile 44 Pin SMT Quad Pak or 40 Pin TDIP
- Analog front end programmable bandwidth
- Extended temperature range –40ºC to +100ºC
- Low power, 645mW
- Low cost, functionally complete

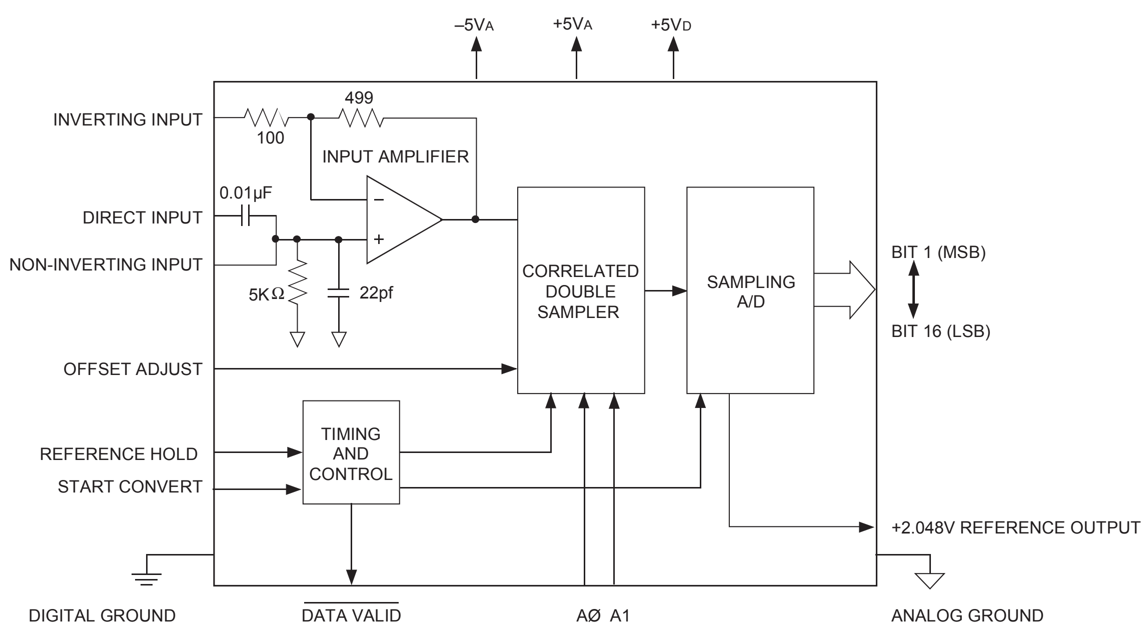
PRODUCT OVERVIEW

The ADCDS-1603 is an application-specific CCD image converter designed for electronic-imaging applications that employ CCD's (charge coupled devices) as their photodetector. The ADCDS-1603 incorporates a "user configurable" input amplifier, a CDS (correlated double sampler) and a 16-bit resolution sampling A/D converter in a single package, providing the user with a complete, high performance, low-cost, low-power, integrated solution.

The key to the ADCDS-1603's performance is a unique, high-speed, high-accuracy CDS circuit, which eliminates the effects of residual charge, charge injection and "kT/C" noise on the CCD's output floating capacitor, producing a pixel data output signal. The ADCDS-1603 digitizes this resultant pixel data signal using a high-speed, low-noise sampling A/D converter.

The ADCDS-1603 requires only the rising edge of start convert pulse to initiate its conversion process and a Reference Hold command to acquire and hold the CCD reference level output. Additional features of the ADCDS-1603 include gain adjust, offset adjust, precision +2.048V reference, and a programmable analog bandwidth function. OVDD selectable 2.5V to 3.3V supply voltage offered in Quad Pak version.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameters	Min.	Typ.	Max.	Units
–5V Supply	–6.5	–	+0.3	Volts
+5V Supply	–0.3	–	+6.5	Volts
OVDD	–0.3	–	+3.8	Volts
Digital Input	–0.3	–	Vdd+0.3V	Volts
Analog Input	–6	–	+6	Volts
Lead Temperature	–	–	300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range, under the following conditions: +5VA = +5V, OVDD = 3.3V, –5VA = –5V, sample rate = 2.3MHz.

Analog Input	Min.	Typ.	Max.	Units
Input Voltage Range (Reference Signal - Pixel data Signal) Gain of 5.99 (INV-IN to GND) Gain of 1 (INV-IN Open)	 – –	 – –	 0.342 2.048	 V p-p V p-p
Input Resistance	–	5000	–	Ohms
Input Capacitance	–	22	–	pF
Digital Inputs				
Logic Levels Logic 1 A0, A1 Logic 0 A0, A1 Logic 1 (REF HLD, START CON) Logic 0 (REF HLD, START CON) **Logic Loading** Logic 1 Logic 0	 4.5 – +2.4 – – –	 – – – – – –	 +Vdd 0.4 – +0.8 +10 -10	 Volts Volts Volts Volts uA uA
Digital Outputs				
Logic Levels Logic 1 (0.5mA) Logic 0 (0.5mA)	 2.8 –	 3.0 –	 3.3 +0.4	 Volts Volts
Logic Levels Logic 1 (0.5mA) Logic 0 (0.5mA)	 4.5 –	 5.0 –	 +0.4	 Volts Volts
Linearity				
Differential Nonlinearity (Histogram, 98kHz) +25°C 0 to 70°C –40 to +100°C	 –0.90 –0.90 –0.98	 ±0.5 ±0.5 ±0.6	 +1.2 +1.2 +2	 LSB LSB LSB
Integral Nonlinearity +25°C 0 to 70°C –40 to +100°C	 – – –	 ±1 ±1 ±2	 – – –	 LSB LSB LSB
Guaranteed No Missing Codes 0 to 70°C –40 to +100°C	 16 16	 – –	 – –	 LSB LSB

Noise	A1	A0	Min.	Typ.	Max.	Units
DC Noise Gain = 1 (INV-IN = NC) ① Start Convert Rate 2.3 MHz	 LO	 LO		 1.7 53		 LSB RMS uV RMS
1.8 MHz	LO	HI		1.5 48		LSB RMS uV RMS
1.0 MHz	HI	LO		1.3 41		LSB RMS uV RMS
800 kHz	HI	HI		1.3 41		LSB RMS uV RMS
DC Noise Gain = 5.99 (INV-IN = GND) ① Start Convert Rate 2.3 MHz	 LO	 LO		 2.5 13		 LSB RMS uV RMS
1.8 MHz	LO	HI		2.0 10.8		LSB RMS uV RMS
1.0 MHz	HI	LO		1.6 8.5		LSB RMS uV RMS
800 kHz	HI	HI		1.6 8.5		LSB RMS uV RMS

Offset/Gain	Min.	Typ.	Max.	Units
Offset Error Gain = 1 +25°C 0 to 70°C –40 to +100°C	 – – –	 0.5 0.5 0.5	 1 1 1.5	 %FSR %FSR %FSR
Gain Error Gain = 1 +25°C 0 to 70°C –40 to +100°C	 – – –	 ±0.5 ±0.5 ±0.5	 ±1 ±1 ±1.5	 %FSR %FSR %FSR
Bandwidth	**Min.**	**Typ.**	**Max.**	**Units**
Input Amplifier –3db BW ⑤ Input Common Mode Voltage Output Voltage Swing	13.5 –3.5 –2.5	– – –	– 3.5 2.5	MHz Volts Volts
Reference				
+25°C	2.038	2.048	2.058	Volts
0 to +70°C	2.038	2.048	2.058	Volts
-40 to +100°C	2.028	2.048	2.068	Volts
Reference Current	–		0.2	mA
Signal Timing ②				
Conversion Rate (–40 to 100°C)	0.001	–	2.3③	MHz
Conversion Time	434	–	–	nSec
Start Convert Pulse Width	300	–	–	nSec

Power Requirements	Min.	Typ.	Max.	Units
Power Supply Range +5V A Supply –5V Supply +5V D Supply ④ OVDD Supply ④	 +4.75 –4.75 –4.75 2.3	 +5.0 –5.0 +5.0 3.3	 +5.25 –5.25 +5.25 3.6	 Volts Volts Volts Volts
Power Supply Currents +5V Supply –5V Supply OVDD Supply	 – – 	 +78 –47 +10	 +83 –52 +12	 mA mA mA
Power Dissipation	–	645	680	mW
Power Supply Rejection (5%) @25°C	–	±0.01	±0.03	%FSR/%V
Environmental				
Operating Temperature Range ADCDS-1603 ADCDS-1603EX	 0 –40	 – –	 +70 +100	 °C °C
Storage Temperature	–65	–	+150	°C
Package Type	40-Pin, TDIP, 2.24"×1.27" FR4 PCB TDIP 44-Pin Quad Pak 0.99"x 0.99"×0.29 LCP Package, FR4 PCB			
Weight	18.1 Grams			
Pin Type	.025 diameter Au Plate, Copper Quad Pak			
Cover (TDIP Package)	Tin Plate Steel			

① See Table 3.
② See Timing Specs, Table 2.
③ See Technical Note: Optimal Performance.
④ +5VD TDIP version, OVDD Quad Pak version. CMOS Output Loading
⑤ A0, A1 = LO

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADCDS-1603 requires careful attention to pc-board layout and power supply decoupling. The device's analog and digital grounds are connected to each other internally. Depending on the level of digital switching noise in the overall CCD system, the performance of the ADCDS-1603 may be improved by connecting all ground pins to a large analog ground plane beneath the package.
2. Bypass all power supplies to ground with a 4.7µf ceramic capacitor in parallel with a 0.1µf ceramic capacitor. Locate the capacitors as close to the package as possible.
3. Offset adjustment resistor (Figure 3), Rext (Figure 2b, 2c, & 2f), and $Rext_1$ & $Rext_2$ (Figure 2d) should be placed as close to the ADCDS-1603 as possible.
4. A0 and A1 (INV-IN = NC) should be bypassed with 0.1µf capacitors to ground to reduce susceptibility to noise.

ADCDS-1603 MODES OF OPERATION

The input amplifier stage of the ADCDS-1603 provides the designer with a tremendous amount of flexibility. The architecture of the ADCDS-1603 allows its input-amplifier to be configured in any of the following configurations:

- Direct Mode (AC coupled)
- Non-Inverting Mode
- Inverting Mode

When applying inputs that are less than 2.048Vp-p, a coarse gain adjustment (applying an external resistor to Inverting Input) must be performed to ensure that the full scale pixel data input signal (saturated signal) produces 2.048Vp-p signal at the input-amplifier's output (V_{OUT}) (See figure 2b & 2C).

In all three modes of operation, the pixel data portion of the signal at the CDS input (i.e. input-amplifier's V_{OUT}) must be more negative than its associated reference level and V_{OUT} should not exceed 2.048Vdc.

The ADCDS-1603 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset error can be reduced to zero using the OFFSET ADJUST feature (See figure 3). For fine gain adjustment model, contact the factory.

DIRECT MODE (AC COUPLED)

This is the most common input configuration as it allows the ADCDS-1603 to interface directly to the output of the CCD with a minimum amount of analog "front-end" circuitry. This mode of operation is used with full-scale pixel data input signals from 0.342Vp-p to 2.048Vp-p.

Figure 2a. describes the configuration for applications using a pixel data input signal with a maximum amplitude of 0.342Vp-p. In this case the input amplifier is configured for the maximum gain of 5.99 (V_{OUT} = 1+(499/100)). All input resistors having a 0.1% tolerance.

Figure 2b. describes the configuration for applications using a pixel data input signal with an amplitude greater than 0.342Vp-p and less than 2.048Vp-p. Using a single external series resistor, the coarse gain of the ADCDS-1603 can be set. The coarse gain of the input amplifier can be determined fron the following equation: V_{OUT} = 2.048Vp-p = V_{IN}* (1+(499/(100+Rext))) (all internal resistors having a 0.1% tolerance).

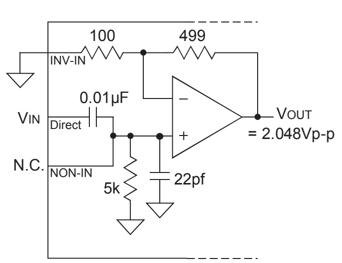


Figure 2a. Direct Mode

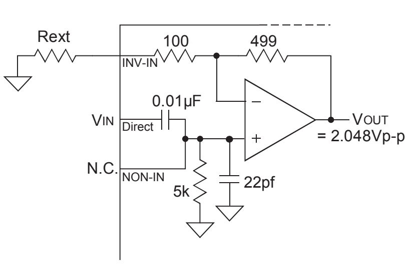


Figure 2b. Direct Mode

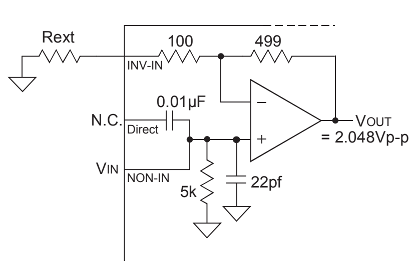


Figure 2c. Non-inverting Mode

Non-Inverting Mode

The non-inverting mode of the ADCDS-1603 allows the designer to either attenuate or add non-inverting gain to the pixel data input signal. This configuration also allows bypassing the ADCDS-1603's internal coupling capacitor, allowing the user to provide an external capacitor of appropriate value.

Figure 2c. describes the typical configuration for applications using pixel data input signals with amplitudes greater than 0.342Vp-p and less than 2.048Vp-p. Using a single external series resistor, the coarse gain of the ADCDS-1603 can be set. The coarse gain of the circuit can be determined from the following equation:

V_{OUT} = 2.048Vp-p = V_{IN}*(1+(499/(100+Rext))),
with all internal resistors having a 0.1% tolerance.

Figure 2d. describes the typical configuration for applications using a pixel data input signal whose amplitude is greater than 2.048Vp-p. Using a single external series resistor (Rext 1) in conjunction with the internal 5K (1%) resistor to ground, an attenuation of the input signal can be achieved. The coarse gain of this circuit can be determined from the following equation:

V_{OUT} = 2.048Vp-p = [V_{IN}*(5000/(Rext1+5000))]*
[1+(499/(100+Rext2))],
with all internal resistors having a 0.1% tolerance.

Inverting Mode

The inverting mode of operation can be used in applications where the analog input to the ADCDS-1603 has a pixel data input signal whose amplitude is more positive than its associated reference level. The ADCDS-1603's correlated double sampler (i.e. input amplifier's V_{OUT}) requires that the pixel data signal's amplitude be more negative than its reference level at all times (see timing diagram for details). Using the ADCDS-1603 in the inverting mode allows the designer to perform an additional signal inversion to correct for any analog "front end" pre-processing that may have occurred prior to the ADCDS-1603.

Figure 2e. describes the typical configuration for applications using a pixel data input signal with a maximum amplitude of 0.342Vp-p. The coarse gain of this circuit can be determined from the following equation:

V_{OUT} = 2.048Vp-p = –V_{IN}*(499/100),
with all internal resistors having a 0.1% tolerance.

Figure 2f. describes the typical configuration used in applications needing to invert pixel data input signals whose amplitude is greater than 0.342Vp-p. Using a single external series resistor, the initial gain of the ADCDS-1603 can be set. The coarse gain of this circuit can be determined from the following equation:

V_{OUT} = 2.048Vp-p = –V_{IN}*(499/100+Rext),
with all internal resistors having a 0.1% tolerance.

Offset Adjustment

Manual offset adjustment for the ADCDS-1603 can be accomplished using the adjustment circuit shown in Figure 3. A software controlled D/A converter can be substituted for the 20KΩ potentiometer. The offset adjustment feature allows the user to adjust the Offset/Dark Current level of the ADCDS-1603 until the output bits are 0000 0000 0000 0000 and the LSB flickers between 0 and 1. The ADCDS-1603's offset adjustment is dependent on the value of the external series resistor used in the offset adjust circuit (Figure 3) and the gain of the input-amplifier.

It should be noted that with increasing amounts of offset adjustment (smaller values of external series resistors), the ADCDS-1603 becomes more susceptible to power supply noise or voltage variations seen at the wiper of the offset potentiometer.

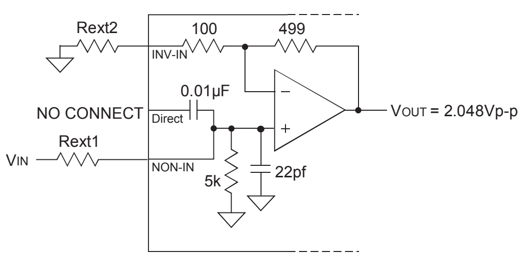


Figure 2d. Non-inverting Mode

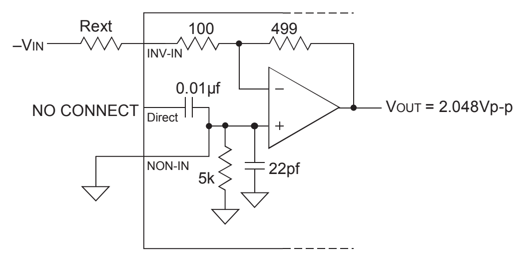


Figure 2f. Inverting Mode

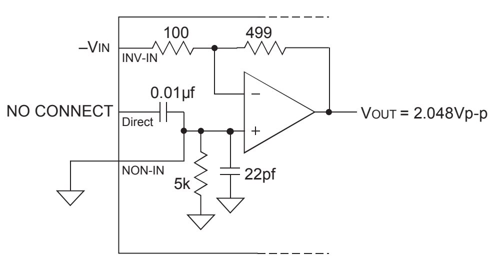


Figure 2e. Inverting Mode

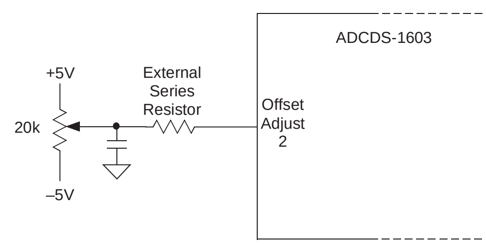


Figure 3. Offset Adjustment Circuit

Fine Gain Adjustment

For fine gain adjustment model, contact the factory.

Output Coding

The ADCDS-1603's output coding is Straight Binary as indicated in Table 1. The table shows the relationship between the output data coding and the difference between the reference signal voltage and its corresponding pixel data signal voltage. Digital circuitry supply uses +5VD for TDIP package version, and OVDD for Quad Pak version. OVDD is a user selectable supply range.

Table 1. Output Coding

Reference – Pixel Data (V)	Scale	Digital Output
>+2.048	>Full Scale	1111 1111 1111 1111
2.048	Full Scale -1LSB	1111 1111 1111 1110
1.536	3/4FS	1111 0000 0000 0000
1.024	1/2FS	1000 0000 0000 0000
0.512	1/4FS	0100 0000 0000 0000
0.256	1/8FS	0010 1000 0000 0000
0.00003125	1LSB	0000 0000 0000 0001
0	0	0000 0000 0000 0000
<0	<0	0000 0000 0000 0000

① Resultant signal from internal CDS (Input to A/D). Assumes Input Amplifier gain set properly. See "Modes of Operation" section.

② The pixel data portion of the differential signal must be more negative than its associated reference level and V_{OUT} should not exceed +2.048V DC.

Optimal Performance

Disturbances to the system while the A/D is undergoing a conversion can result in degradation of performance. It is therefore recommended that both digital and analog signals (including the Reference/Pixel data inputs to the ADCDS) not be allowed to switch during a time window of 50ns to 300ns following the rising edge of the Start Convert command when operating in the 0°C to 70°C temperature range. For extended temperature range devices it may be required to have no signals switching until after 300ns. See timing Figure 7 "A/D Critical Conversion Window."

While an ongoing conversion is in process the ADCDS-1603 is susceptible to disturbances that could affect the quality of the conversion process. This period of time would be the first 300ns following the rising edge of the Start Convert command.

Note that the internal A/D of the ADCDS-1603 is performing the conversion process during the 300ns immediately following the rising edge of the Start Convert signal. Disturbances to the device during this time can result in a degradation of the quality of the conversion. Therefore, it may be necessary to assure that no digital or analog signals be allowed to switch during this time period. In this case, acquisition and settling limitations may require that the overall conversion rate of the ADCDS-1603 be reduced.

Note: At initial power-up, the first 186 conversions should be ignored.

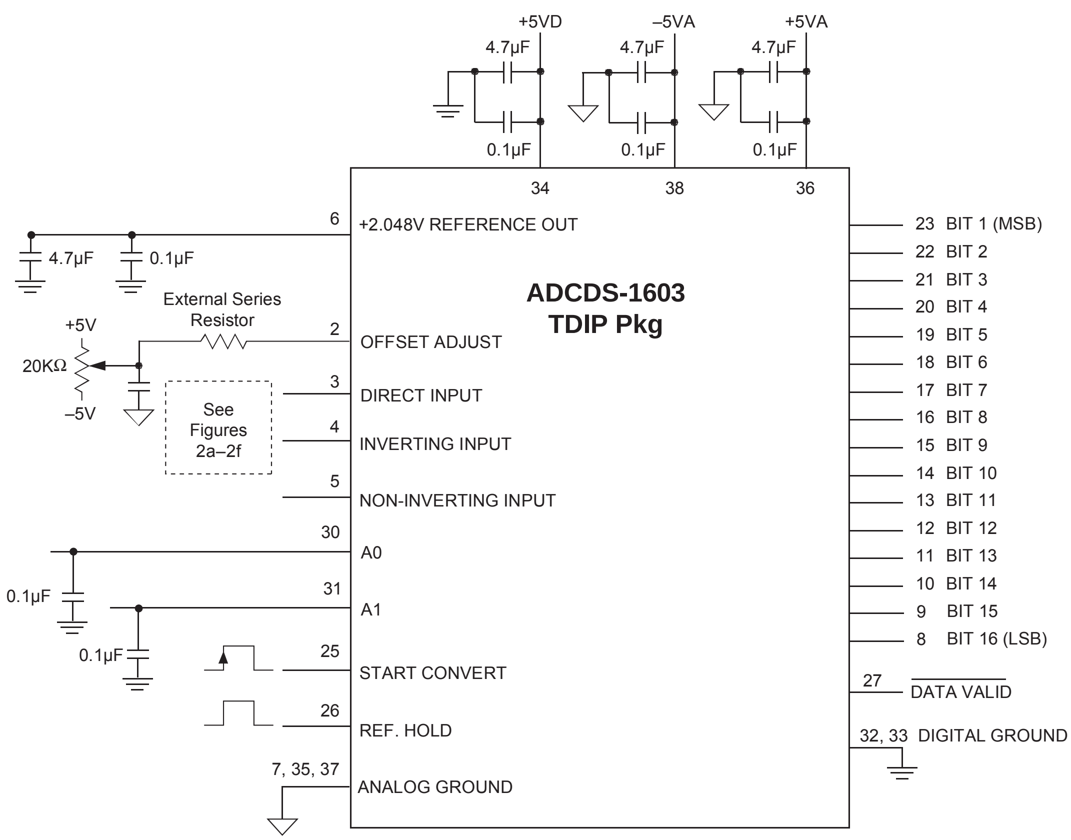


Figure 6A. ADCDS-1603 TDIP Pkg Connection Diagram

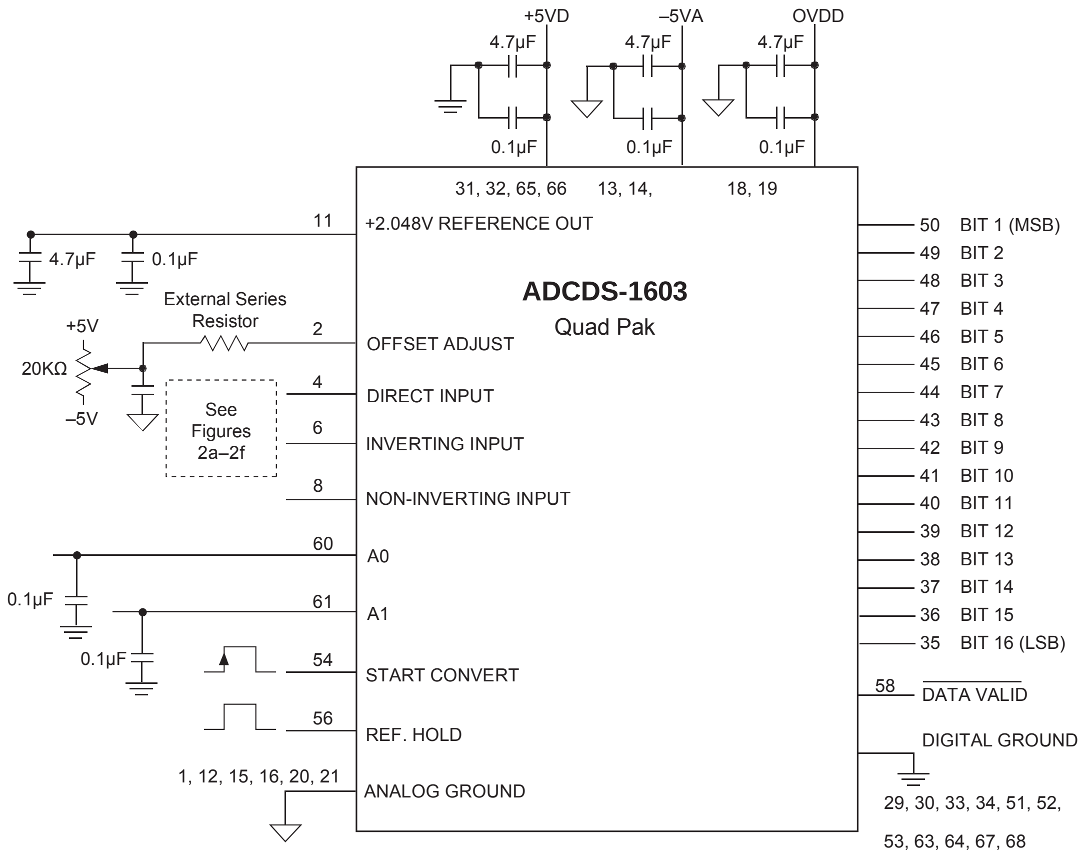


Figure 6B. ADCDS-1603 L Quad Pak Connection Diagram

Programmable Analog Bandwidth Function

When interfacing to CCD arrays with very high-speed "read-out" rates, the ADCDS-1603's input stage must have sufficient analog bandwidth to accurately reproduce the output signals of the CCD array. The amount of analog bandwidth determines how quickly and accurately the "Reference Hold" and the "CDS output" signals will settle ③. If only a single analog bandwidth was offered, the ADCDS-1603's bandwidth would be set to acquire and digitize CCD output signals to 16-bit accuracy, at the maximum conversion rate of 2.3MHz (434ns see Figure 8 for details). Applications not requiring the maximum conversion rate would be forced to use the full analog bandwidth at the possible expense of noise performance.

Table 2. Timing Specification ③

Parameters	Symbol③	Min.	Typ.	Max.	Units
2.3 MHz Conversion					
Conversion Time	T1	–	434	3	ns
A0		–	LO	–	
A1		–	LO	–	
Reference Acquisition Time	T2	–	180	–	ns
Pixel Data Settling Time	T3	–	120	134	ns
Start Convert	T4	300	–	–	ns
1.8 MHz Conversion					
Conversion Time	T1	–	555	–	ns
A0		–	HI	–	
A1		–	LO	–	
Reference Acquisition Time	T2	–	230	–	ns
Pixel Data Settling Time	T3	–	205	–	ns
Start Convert	T4	300	–	–	ns
1 MHz Conversion					
Conversion Time	T1	–	1000	–	ns
A0		–	LO	–	
A1		–	HI	–	
Reference Acquisition Time	T2	–	370	–	ns
Pixel Data Settling Time	T3	–	520	–	ns
Start Convert	T4	300	–	–	ns
800 kHz Conversion					
Conversion Time	T1	–	1250	–	ns
A0		–	HI	–	
A1		–	HI	–	
Reference Acquisition Time	T2	–	470	–	ns
Pixel Data Settling Time	T3	–	680	–	ns
Start Convert	T4	300	–	–	ns

③ See timing figures 7 and 8.

The ADCDS-1603 avoids this situation by offering a fully programmable analog bandwidth function. The ADCDS-1603 allows the user to "bandwidth limit" the input stage in order to realize the highest level of noise performance for the application being considered. Table 2 describes recommendations in selecting the appropriate reference hold (Reference Aquisition Time) and CDS output (Pixel Data Settling Time) needed for a particular application. Each of the selections listed in the Noise section of Functional Specifications have been optimized to provide only enough analog bandwidth to acquire a full scale input step (Vsat), to 16-bit accuracy, in a single conversion. Increasing the analog bandwidth (using a faster settling and acquisition time) would only serve to potentially increase the amount of noise at the ADCDS-1603's output. The ADCDS-1603 uses a two bit digital word to select four different analog bandwidths for the ADCDS-1603's input stage (See Table 2 for details). Functional Specifications show typical RMS noise for given bandwidth and gain settings.

Timing

The ADCDS-1603 requires two independently operated signals to accurately digitize the analog output signal from the CCD array.

- Reference Hold
- Start Convert

The "Reference Hold" signal controls the operation of the internal correlated double sampler (CDS) circuit. A logic "1" capture the value of the CCD's reference signal. The Reference Hold Signal allows the user to control the exact moment when the internal CDS is placed into the "hold" mode. For optimal performance the internal CDS should be placed into the "hold" mode once the reference signal has fully settled from all switching transients to the desired accuracy (t_2).

Note that while an ongoing conversion is in process the ADCDS-1603 is susceptible to disturbances that could affect the quality of the conversion process. This period of time would be the first 300ns following the rising edge of the Start Convert command.

Note that the internal A/D of the ADCDS-1603 is performing the conversion process during the 300ns immediately following the rising edge of the Start Convert signal. Disturbances to the device during this time can result in a degradation of the quality of the conversion. Therefore, it may be necessary to assure that no digital or analog signals be allowed to switch during this time period. In this case, acquisition and settling limitations may require that the overall conversion rate of the ADCDS-1603 be reduced.

Once the reference signal has been "held" and the pixel data portion of the CCD's analog output signal appears at the ADCDS-1603's input, the internal correlated double sampler produces a "CDS Output" signal (see Figure 8.) which is the difference between the "held" reference level and its associated pixel data level (Reference-Pixel Data). When the "CDS Output" signal has settled to the desired accuracy (t_3), the A/D conversion process can be initiated with the rising edge of the Start Convert signal.

Once the A/D conversion has been initiated, the Reference Hold can be placed back into the "Acquisition" mode in order to begin aquiring the next reference level. For optimal performance the ADCDS-1603's should be placed back into the "Aquisition" mode (Reference Hold to logic "0") during the CCD's "Reference Quiet Time" ("Reference Quiet Time" is defined as the period when the CCD's reference signal has settled from all switching transients to the desired accuracy (see Figure 7.) Placing the sample-hold back into the "aquisition" mode during the "Reference Quiet Time" prevents the ADCDS-1603's internal amplifiers from unnecessarily tracking (reproducing) the reset feedthrough glitch that occurs during the CCD's reset to reference transition.

Disturbances to the system while the A/D is undergoing a conversion can result in degradation of performance. It is therefore recommended that both digital and analog signals (including the Reference/Pixel data inputs to the ADCDS) not be allowed to switch during a time window of 50ns to 300ns following the rising edge of the Start Convert command when operating in the 0°C to 70°C temperature range. For extended temperature range devices it may be required to have no signals switching until after 300ns. See timing Figure 7 "A/D Critical Conversion Window."

Note: At initial power-up, the first 186 conversions should be ignored.

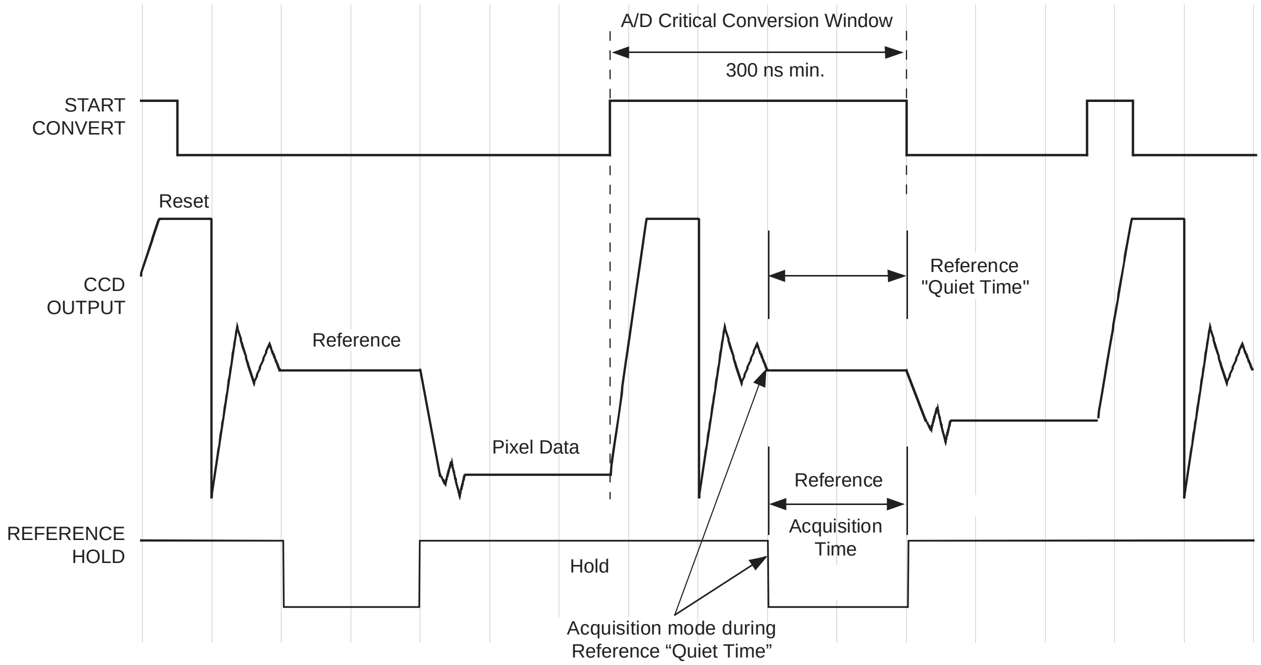
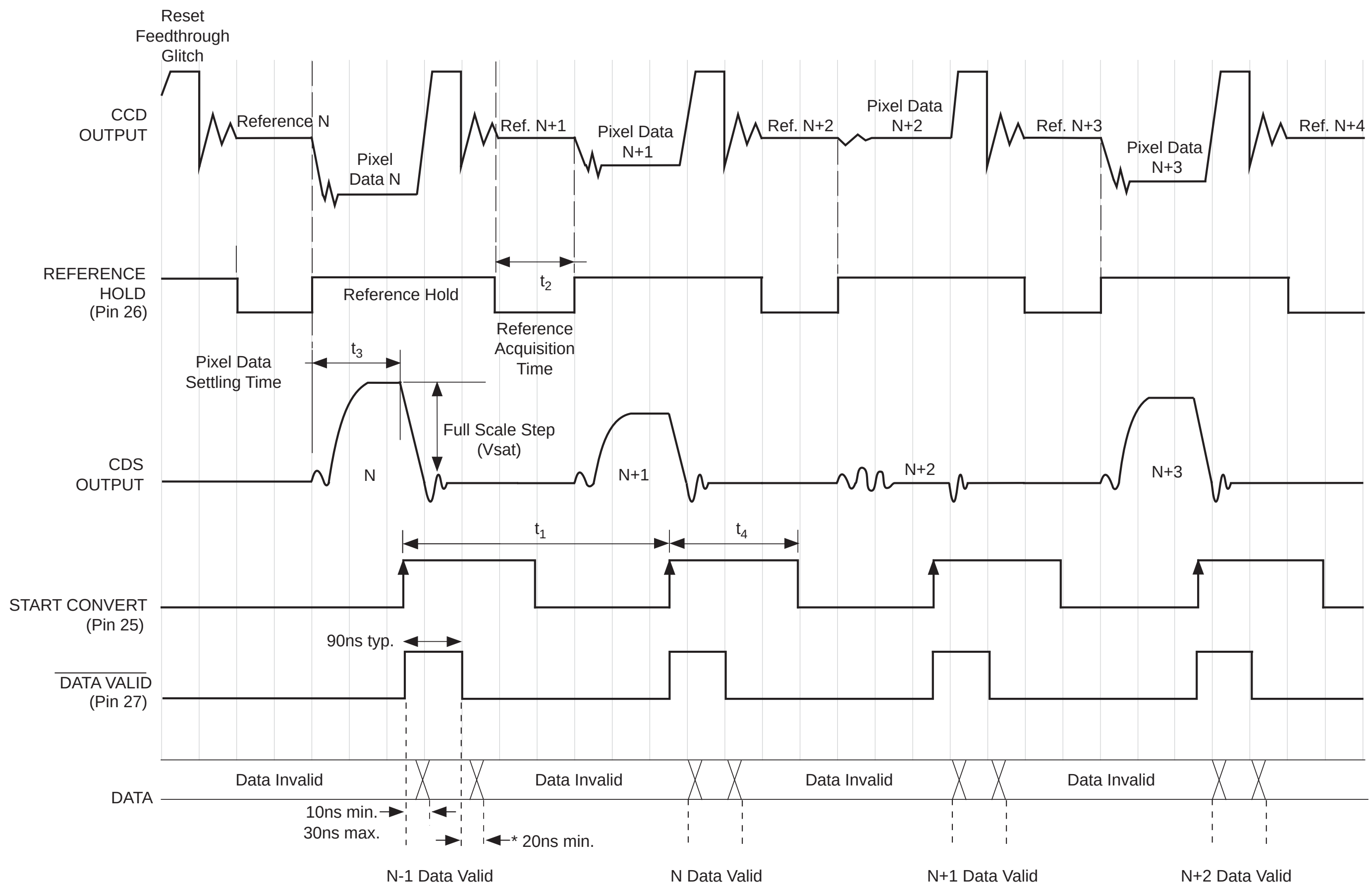


Figure 7. Reference Hold Timing



* Output Data guaranteed to remain valid a minimum of 20ns after falling edge of DATA VALID.
++ CDS Output captured by S/H at rising edge of Start Convert.

Figure 8. ADCDS-1603 Timing Diagram

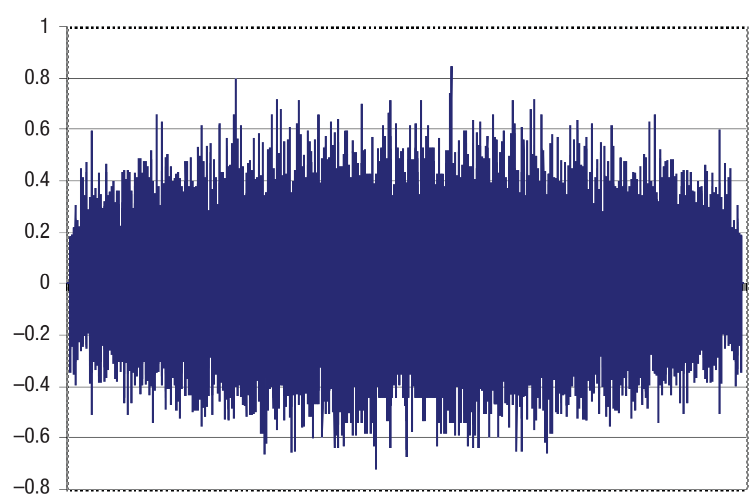
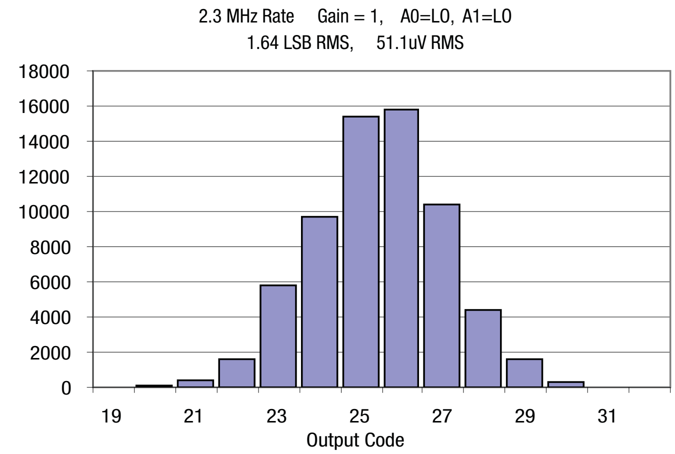
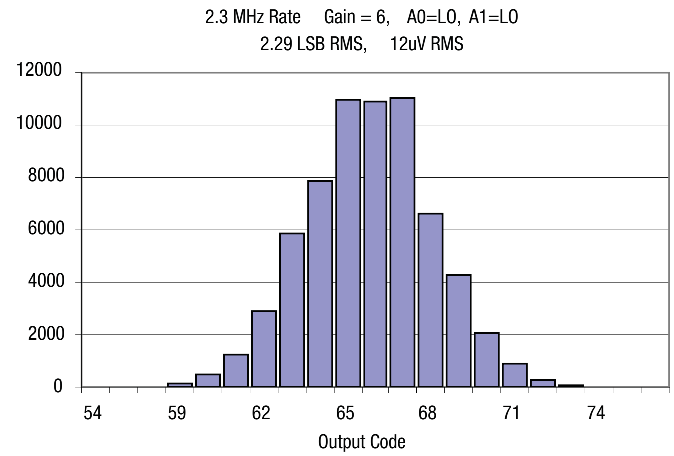


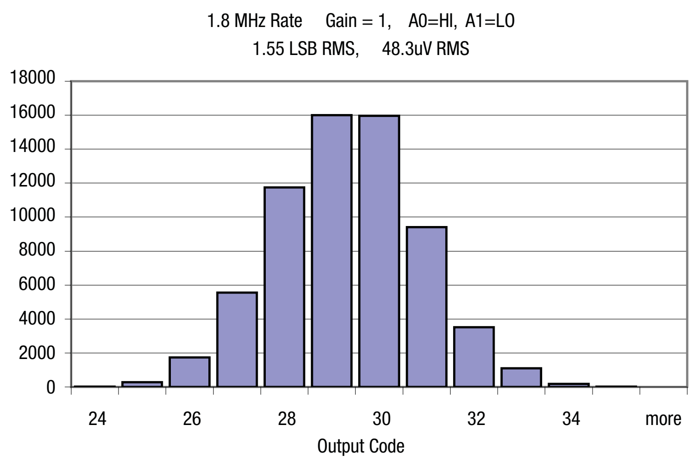
Figure 9. ADCDS-1603 Differential Nonlinearity, LSBs

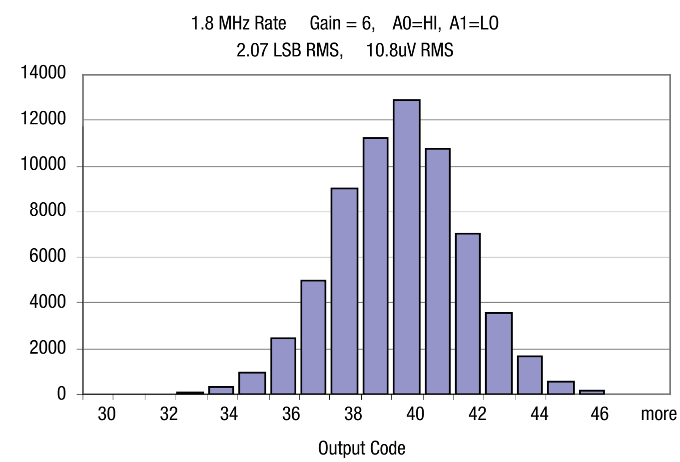
ADCDS-1603 Grounded Input Histogram – 2.3 MHz Rate



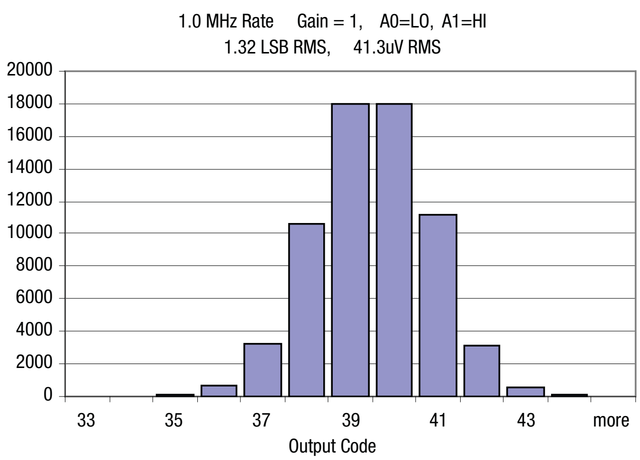


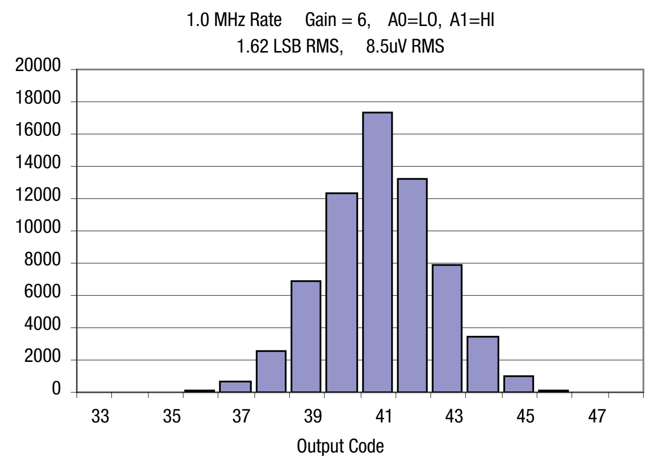
ADCDS-1603 Grounded Input Histogram – 1.8 MHz Rate



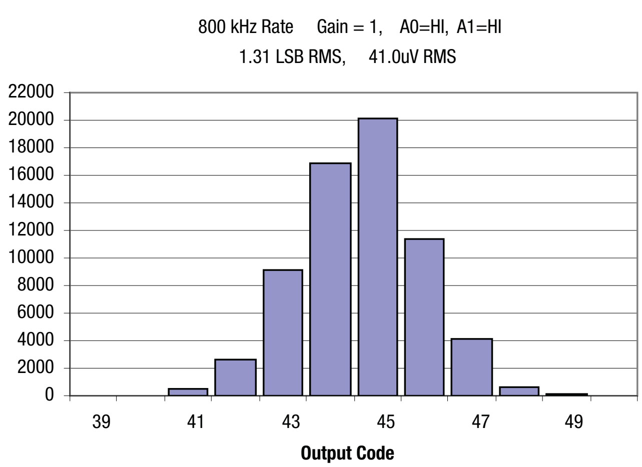


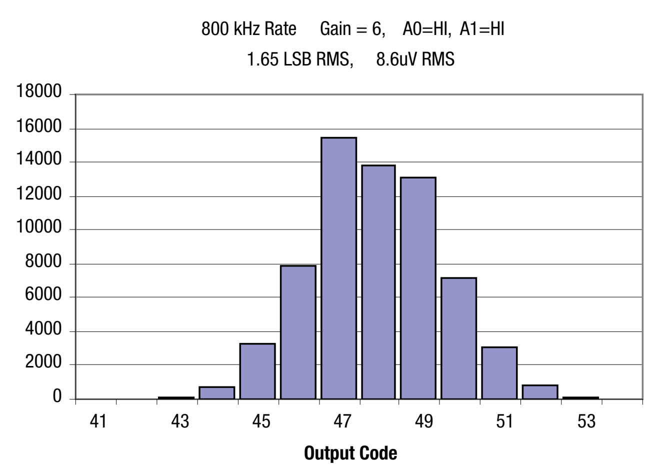
ADCDS-1603 Grounded Input Histogram – 1.0 MHz Rate



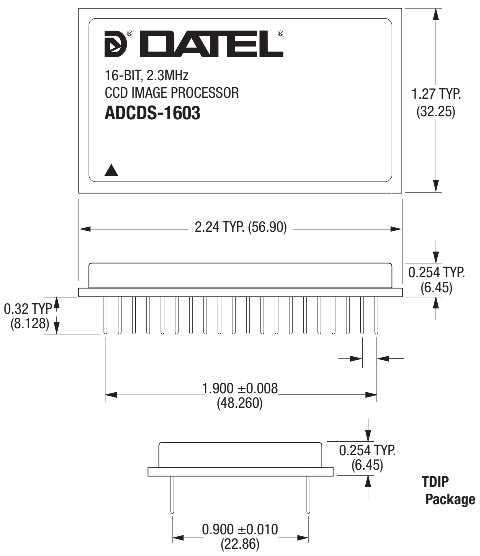


ADCDS-1603 Grounded Input Histogram – 800 MHz Rate

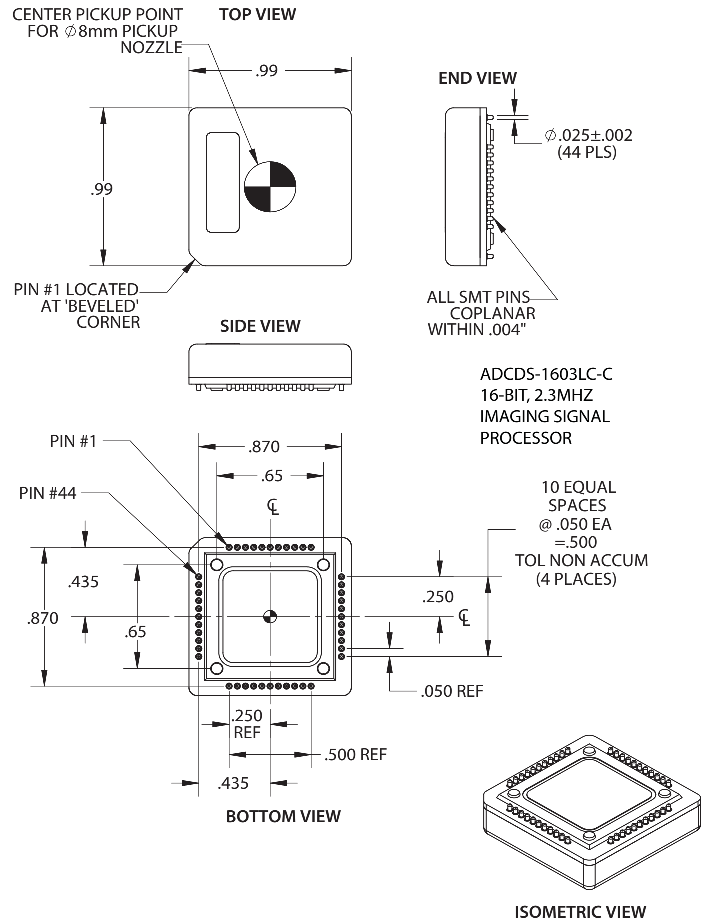




MECHANICAL DIMENSIONS inches (mm)



TDIP Package



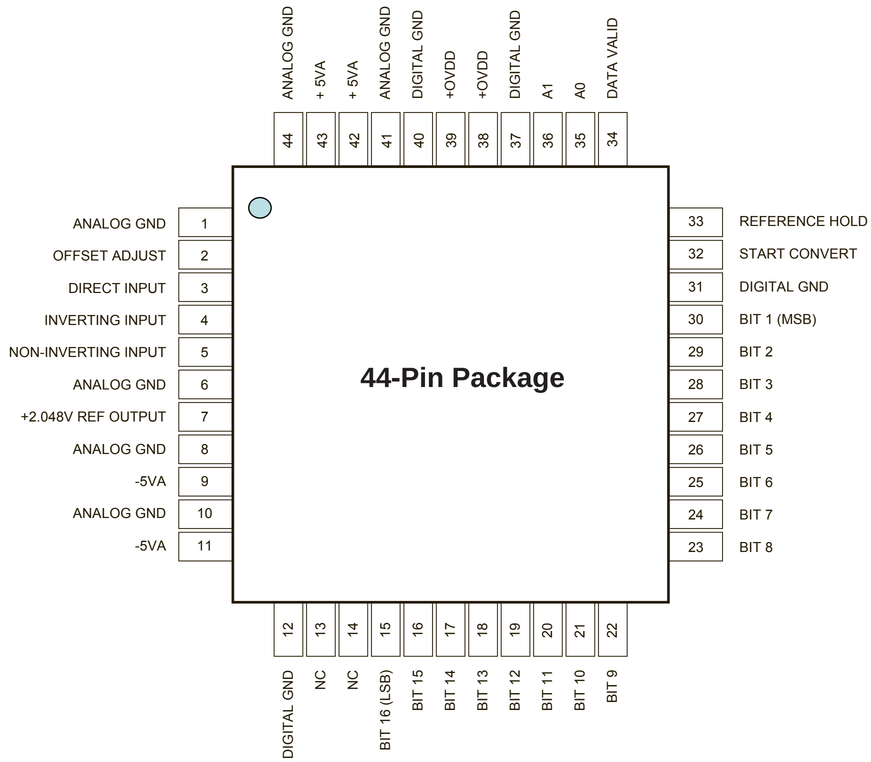
Quad Pak

ORDERING INFORMATION					
MODEL NUMBER	OPERATING TEMP. RANGE	PACKAGE	ROHS	ACCESSORIES	
ADCDS-1603	0 to +70°C	TDIP	No	ADCDS-B1801L-C / ADCDS-B1603L-C EVAL BD.	Evaluation Board (without ADCDS-1603)
ADCDS-1603EX	–40 to +100°C	TDIP	No		
ADCDS-1603-C	0 to +70°C	TDIP	Yes		
ADCDS-1603EX-C	–40 to +100°C	TDIP	Yes		
ADCDS-1603LC-C	0 to +70°C	Quad Pak	Yes		
ADCDS-1603LEX-C	–40 to +100°C	Quad Pak	Yes		

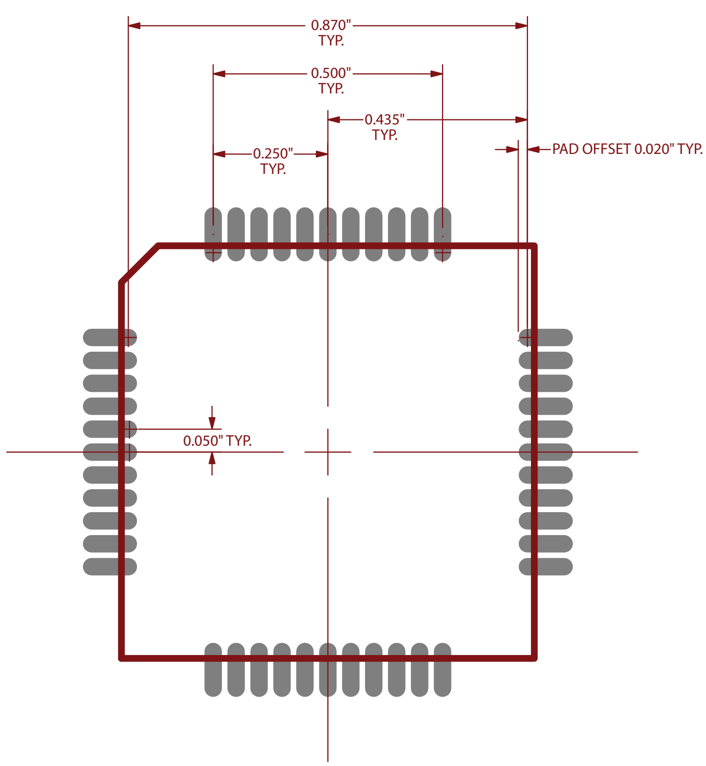
INPUT/OUTPUT CONNECTIONS— ADCDS-1603 TDIP Package

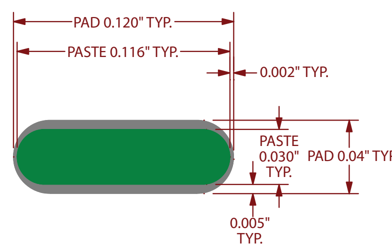
PIN	FUNCTION	PIN	FUNCTION
1	NO CONNECTION	40	NO CONNECTION
2	OFFSET ADJUST	39	NO CONNECTION
3	DIRECT INPUT	38	–5VA
4	INVERTING INPUT	37	ANALOG GROUND
5	NON-INVERTING INPUT	36	+5VA
6	+2.048V REF. OUTPUT	35	ANALOG GROUND
7	ANALOG GROUND	34	+5VD
8	BIT 16 (LSB)	33	DIGITAL GROUND
9	BIT 15	32	DIGITAL GROUND
10	BIT 14	31	A1
11	BIT 13	30	AØ
12	BIT 12	29	NO CONNECTION
13	BIT 11	28	NO CONNECTION
14	BIT 10	27	DATA VALID
15	BIT 9	26	REFERENCE HOLD
16	BIT 8	25	START CONVERT
17	BIT 7	24	NO CONNECTION
18	BIT 6	23	BIT 1 (MSB)
19	BIT 5	22	BIT 2
20	BIT 4	21	BIT 2

INPUT/OUTPUT CONNECTIONS—ADCDS-1603LEX-C 44-Pin Quad Pak



RECOMMENDED FOOTPRINT—ADCDS-1603LEX-C 44-Pin Quad Pak

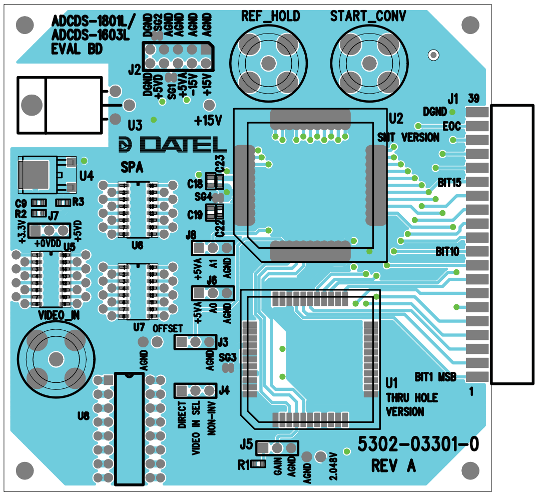




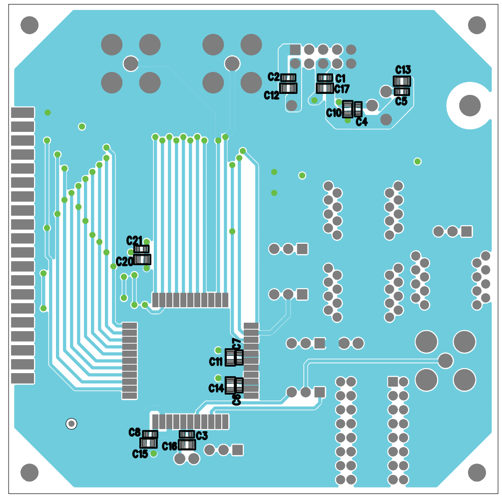
RECOMMENDED PAD AND PASTE DIMENSIONS

EVALUATION BOARD

ASSEMBLY



TOP VIEW



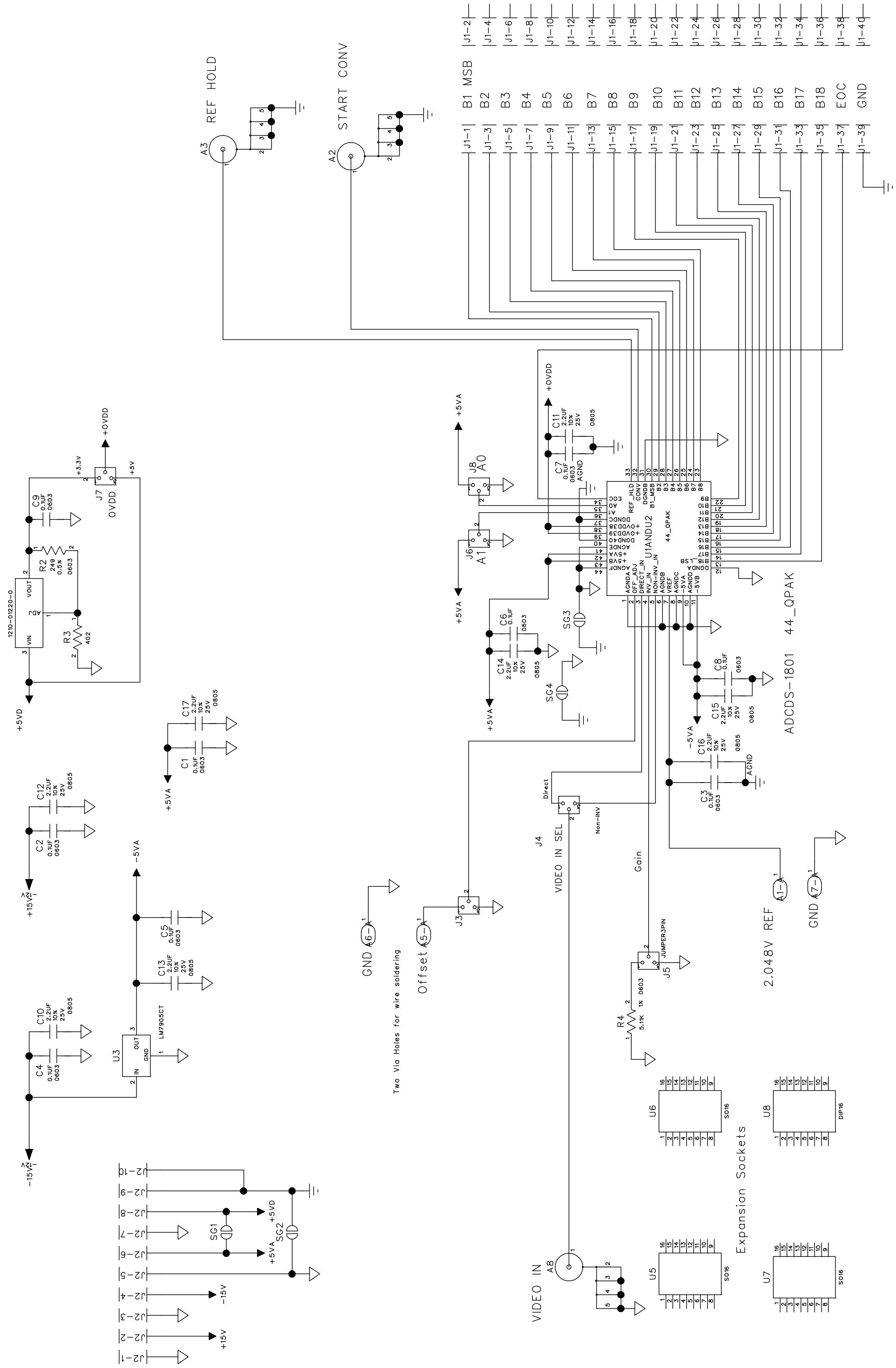
BOTTOM VIEW

BOM

Rev.	Title	QPA	Ref Des
1	ADCDS-B1801L-C/ADCDS-B1603L-C EVAL BD ASSY DWG		
1	ADCDS-B1801L-C/ADCDS-B1603L-C EVAL BD SCH DWG		
1	PCB ADCDS-B1801L-C/ADCDS-B1603L-C EVALUATION BOARD	1	
N/A	IC LIN TO220 NEG VOLT REG 15V 7905C	1	U3
N/A	IC ANA SMT VREG ADJ SINGLE 317 19.1V 4% DPAK INDUSTRIAL 125C	1	U4
N/A	CAP SMT NON POL CERAMIC X7R 0.1UF 50V 10% 0603 STANDARD	9	C1, C2, C3, C4, C5, C6, C21, C22, C23
N/A	CAP SMT NON POL CERAMIC X7R 2.2UF 25V 10% 0805 STANDARD	11	C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20
N/A	RES SMT FXD THICK FILM STANDARD 402R 1% 0603 100MW	1	R3
N/A	RES SMT FXD THICK FILM STANDARD 5.11K 1% 0603 100MW	1	R1
N/A	RES SMT FXD THIN FILM STANDARD 249R 0.5% 0603 100MW	1	R2
N/A	CON OTHER JUMPER 0.1IN 3A	6	J3, J4, J5, J6, J7, J8
N/A	CON PTH CONTACT PIN PRESSFIT 3A 0.04IN	18	USE W/J3, J4, J5, J6, J7, J8
N/A	CON PTH COAX BNC PCB RECEPT 0DEG	3	
N/A	ENGLISH STANDOFF HEX ALUMINIUM 4-40 0.5IN	4	
N/A	SCREW MACHINE CARB STEEL PAN HD PHILLIPS #4-40 X .250 LONG	4	

EVALUATION BOARD

SCHEMATIC



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