ADS-424 / ADS-429

12-Bit, 250kHz, Single-ended and Differential Inputs, Multi Channel SAR A/D Converters

FEATURES

- Multi- channel 250kSPS
- 12-bit resolution
- Single-ended and fully differential, rail-rail inputs
- Humidity and stress resistant ceramic LCC package for -QL and /883 models
- -40°C to +105°C and -55°C to +125°C operating temperature ranges
- 100% testing over temperature
- High-Rel process flow, burn-in, environmental, lot and ATE traceability
- No missing codes over specified temperature range
- SPI compatible serial interface
- THD -86dB
- 2.7V to 5.25 operating supply voltage range
- 3mA operating supply current 8µA power-down current
- Small, 16-pin, TSSOP or ceramic LCC package
- Pb-Free (Rohs compliant)

PRODUCT OVERVIEW

The ADS-424 and ADS-429 are 12 bit multi-channel SAR Analog to Digital converters housed in TSSOP or ceramic LCC packages. The ADS-424 offers four differential input channels while the ADS-429 offers eight single -ended input channels.

Both designs contain a 12-bit, 250kSPS SAR Analog to Digital Converter that delivers excellent integral and differential linearity performance over changes in both supply voltage and temperature. With high-impedance, rail to rail inputs, the ADS-424 and ADS-429 are ideal selections for low power and battery operated multi-channel data acquisition systems. The A/D is designed to accept an external reference voltage while operating over a supply voltage range of +2.7V to +5.25V.

These products are offered in either a small 16 pin TSSOP plastic package or a fully hermetic sealed ceramic LCC package for High-Rel or military applications. The hermetic ceramic package, offered for the –QL and /883 versions, protects the IC from the effects of moisture and outgassing making the precision DC characteristics of the ADC more stable in environments where humidity is a concern. In addition, the LCC package isolates the IC from the stresses that may occur on the printed circuit board caused by variations in temperature.

Employing a serial SPI compatible digital interface, this device requires only 3mA of operating supply current and a mere 8µA during power-down mode. The TSSOP package models are drop in compatible with several industry standard converters.

DATEL offers these converters fully tested over temperature with ATE results recorded and stored for the operating temperature ranges of -40°C to +105°C (Enhanced) or –55°C to +125°C (military). Burn-in and environmental screening are also available.

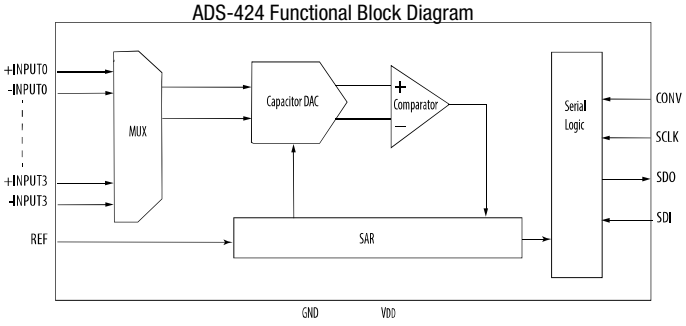
Products are offered in military temperature grades as well as fully screened High-Reliability -QL and /883 models.

APPLICATIONS

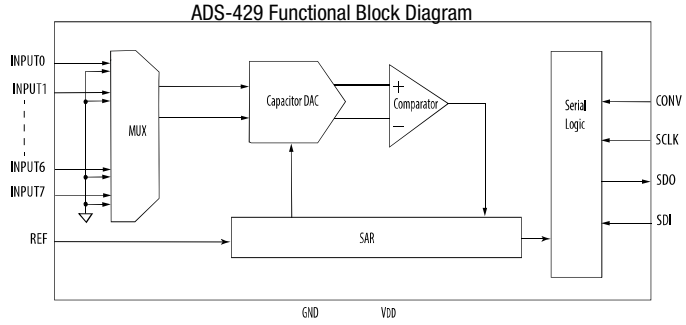
- Multi- channel data acquisition systems
- MIL-STD/883 applications
- Defense / aerospace multi- channel systems
- Low-power Data Acquisition
- Flow control, Pressure sensors
- Scientific test instruments
- Industrial process control
- Instrumentation measurement
- Battery-powered handheld equipment

BLOCK DIAGRAM / PINOUTS

ADS-424 Functional Block Diagram



ADS-429 Functional Block Diagram



ADS-424 PINOUT			
PIN	PIN NAME	PIN	PIN NAME
1	V_{DD}	16	CONV
2	GND	15	SCLCK
3	REF	14	SDO
4	GROUND	13	SDI
5	+INPUT0	12	+INPUT3
6	-INPUT0	11	-INPUT3
7	+INPUT1	10	+INPUT2
8	-INPUT1	9	-INPUT2

ADS-429 PINOUT			
PIN	PIN NAME	PIN	PIN NAME
1	V_{DD}	16	CONV
2	GND	15	SCLCK
3	REF	14	SDO
4	GROUND	13	SDI
5	INPUT0	12	INPUT7
6	INPUT1	11	INPUT6
7	INPUT2	10	INPUT5
8	INPUT3	9	INPUT4

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ADS-424 / ADS-429

12-Bit, 250kHz, Single-ended and Differential Inputs, Multi Channel SAR A/D Converters

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
Analog Inputs referenced to GND	-0.3 to V_{DD} +0.3	V
VREF referenced to GND	-0.3 to V_{DD} +0.3	V
Digital Inputs referenced to GND	-0.3 to V_{DD} +0.3	V
V_{DD} (pin 8) to GND (4)	-0.3 to +6.0	V
ESD Human Body Model	5	kV

PHYSICAL / ENVIRONMENTAL		
PARAMETERS	LIMITS	UNITS
θjc TSSOP package	29	°C/W
θca TSSOP package	92	°C/W
Storage Temperature Range	-65 to +150	°C

FUNCTIONAL SPECIFICATIONS [1]

V_{DD} = 2.7V to 5V, $V_{REF} = V_{DD}$, $V_{CM=} V_{DD}/2$, F_{SCLK} 20MHz @ 25°C unless otherwise specified.

ANALOG INPUTS	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Input Voltage Range[1]					
INPUT+	VCM = VREF	—	VCM ± VREF/2	—	V
INPUT-	VCM = VREF	—	VCM ± VREF/2	—	V
Input Leakage Current		-1	687	+1	µA
Input Capacitance	Track Mode	—	14	—	pF
Input Capacitance	Hold Mode	—	5	—	pF
STATIC PERFORMANCE					
Resolution		—	12	—	Bits
Integral Nonlinearity		-0.7	±0.5	+0.7	LSB
Differential Nonlinearity (Fin = 10kHz)		-0.7	±0.5	+0.7	LSB
Offset Error		–6	—	+6	LSB
Offset Error Channel-Channel Matching		-2		+2	LSB
Gain Error		–6	—	+6	LSB
Gain Error Channel-Channel Matching		-2		+2	LSB
No Missing Codes		12	—	—	Bits
DYNAMIC PERFORMANCE					
Peak Harmonics (Fin = Full scale – 0.1dB @ 20kHz)					
Single-ended Inputs		—	96	—	dB
Differential Inputs		—	96	—	dB
Total Harmonic Distortion (Fin = Full scale – 0.1dB @ 10kHz)		—	—	—	
Single-ended Inputs		—	-86	—	dB
Differential Inputs		—	-86	—	dB
Signal-to-Noise Ratio (Fin = Full scale – 0.1dB @ 10kHz)					
Single-ended Inputs		—	73.4	—	dB
Differential Inputs		—	73.4	—	dB
Signal-to-Noise Ratio & distortion (Fin = Full scale – 0.1dB @ 10kHz)					
Single-ended Inputs		—	73.1	—	dB
Differential Inputs		—	73.1	—	dB
Input Bandwidth (–3dB)		—	2.5	—	MHz
Aperture Delay Time		—	12	—	ns
Aperture Uncertainty		—	25	—	ps-rms
S/H Acquisition Time to ±0.001% of FSR		—	—	400	ns
REFERENCE					
External Reference Input Voltage		2	2.5	V_{DD}	V
Reference Input Current		—	200	220	µA
Reference Input Capacitance		—	10	—	pf
DIGITAL INPUTS					
Logic Levels					
Logic "1"		0.7 x V_{DD}	—	—	V
Logic "0"		—	—	0.2 x V_{DD}	V
Logic Loading "1"		-100	—	+100	nA
Logic Loading "0"		-100	—	+100	nA

DIGITAL OUTPUTS					
Logic Levels					
Logic "1"	I OUT = 1 mA	V_{DD}-0.4	—	—	V
Logic "0"	I OUT = - 1 mA	—	—	0.2 x V_{DD}	V
Output Coding					
Single-ended Inputs		Binary			
Differential Inputs		Two's Complement			
TIMING (cont.)		**MIN.**	**TYP.**	**MAX.**	**UNITS**
Conversion time t_{CONV}		—	—	900	ns
A/D Conversion Rate		1	—	—	MHz
Serial Clock Period t_{SCLK}		60	—	—	ns
Serial Clock Pulse width t_{SW}		0.4 x t_{SCLK}	—	0.6 x t_{SCLK}	ns
Serial Clock Frequency FSCLK		0.01	—	18	MHz
Chip Select (CS) Pulse Width HI t_{CSW}		10	—	—	ns
Chip Select (CS) Falling Edge to SCLK Falling Edge t_{CSdly}		10	—	—	ns
Chip Select (CS) Falling Edge to SDO Valid t_{CSDO}		—	—	20	ns
Serial Clock SCLK Falling Edge to SDO Valid t_{SCLKDV}		—	—	40	ns
Serial Clock SCLK Falling Edge to SDO Hold t_{SDH}		10	—	—	ns
Serial Clock SCLK Falling Edge to SDO Disable Time $t_{DISABLE}$		10	—	40	ns
Quiet Time Before Sample t_{QUIET}		60	—	—	ns
POWER REQUIREMENTS	**TEST CONDITION**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Power Supply Ranges					
V_{DD} Supply Voltage		2.7	—	5.25	V
V_{DD} Supply Current		—	3	3.5	mA
V_{DD} Supply Current	Auto Power Down	—	8	50	µA
V_{DD} Supply Current	Auto Sleep	—	0.4	—	mA
Power Dissipation	Conversion Mode	—	15	17.5	mW
Power Supply Rejection		—	70	—	dB
OPERATING TEMPERATURE		**MIN.**	**TYP.**	**MAX.**	**UNITS**
SE models		-40	—	+105	°C
SM models		-55	—	+125	°C
-QL models		-55	—	+125	°C
/883 models		-55	—	+125	°C
PACKAGE TYPE		**MIN.**	**TYP.**	**MAX.**	**UNITS**
SE, SM models		16-pin TSSOP			
-QL, /883 models		Hermetic, Ceramic LCC			

NOTES:

1. Voltage applied to ±VIN must be between GND and V_{DD}.
2. θj measured on thermally conductive test card in free air.
3. Exceeding maximum conversion rate (minimum acquisition time not met) may require power recycle to restore A/D to normal operation.
4. Note that voltage applied to REF should not exceed V_{DD} by more than 100mV or the ESD protection diodes will forward bias and degrade A/D accuracy.

TECHNICAL NOTES

Theory of Operation

The ADS-424 and ADS-429 are 12-bit multi-channel SAR A/D converters housed in a 16-pin TSSOP of ceramic LCC package. The ADS-424 is a 4-channel with differential inputs while the ADS-429 offers 8-channels with single-ended inputs.

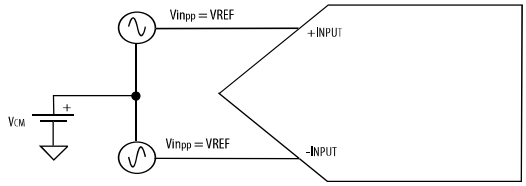
These converters perform successive approximation conversion using capacitive charge redistribution. An internal oscillator provides the master clock for the successive approximation conversion. The process involves two steps: the acquisition mode and the redistribution mode where the actual A/D conversion takes place. The acquisition mode is initiated by the CONV signal going to a logic low where the analog inputs are switched to charge binary weighted capacitors. The CONV signal must remain low for the specified amount of acquisition time to allow the binary capacitors to be charged to the appropriate accuracy. During the conversion mode the binary weighted capacitors are disconnected from the input and switched to an internal comparator where they are sequentially switched from MSB to LSB referencing them to an internal reference voltage. The comparator compares the charge of each weighted capacitor to provide a serial 12 bit digital output.

An internal register, accessed using the SCLCK and SDI control lines, allows the user to select the desired input channel, to configure the internal register to export its contents along with the associated data conversion output word , and to activate a feature whereby the A/D is powered down between conversions.

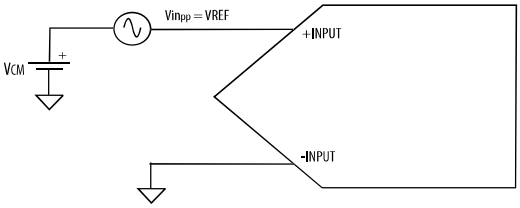
Differential and Single-ended Analog Inputs

The ADS-424 has fully differential input with a full scale range equal to two times the voltage of REF (pin 3). As seen in Figure 2 below, the signals present at the +INPUT and -INPUT are 180°out of phase and have a peak-to-peak amplitude equal to V_{REF}. Because these signals are out of phase the full-scale range of the A/D becomes 2 x V_{REF}, effectively doubling the input range over a single-ended topology. As a result, the dynamic range of the A/D is doubled resulting in improved harmonic distortion as well as noise performance.

The ADS-429 offers 8 single-ended inputs with a full scale range equal to the voltage of V_{REF}. The common mode voltage of the input signals must be such that it assure that voltage swing on +INPUT and -INPUT remain within the operating range of the A/D.



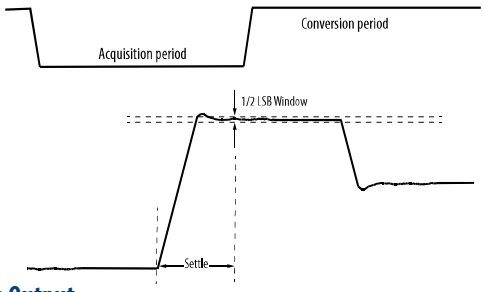
Differential Input



Single-ended Input

Input Multiplexer

The analog input is connected to the A/D section through the input multiplexer circuit. Channel selection is controlled by writing to the internal register via the SCLCK and SDI control lines. The specified acquisition time encompasses the time required for both the multiplexer and the A/D's binary weighted sampling circuit to settle to the specified 12 bit accuracy.



Data Output

SDO data is read during the conversion period of the data conversion process (see timing diagram). The A/D goes into an idle period between the conversion and acquisition periods. Bringing the CONV signal low during the idle period initiates the acquisition mode. After the appropriate acquisition time the CONV is pulsed high for a minimum of 100ns and then brought low again. The A/D is now prepared for the transfer of both SDI and SDO data. In order to minimize the corruption of an ongoing conversion from the effects of digital data transfer, all data transfer must be completed within the "tdata" specified time after the CONV goes low. The final SCLCK pulse transitions the SDO to a high-impedence state.

When the conversion is complete the internal logic circuitry will assert the SDO to a logic low indicating that the conversion is complete. This low-going signal may be used as an interrupt to begin a new acquisition phase. In order to avoid loss of data, the SDO must be read prior to initiation of another conversion.

Serial data output (SDO) is provided in an MSB to LSB format as Two's Complement for differential input devices and as Straight Binary for single-ended devices.

OUTPUT CODING : DIFFERENTIAL INPUT MODELS		
INPUT	VOLTAGE *(+INPUT) - (-INPUT)*	TWO'S COMPLEMENT CODING MSB LSB
+FS	+VREF	0111 1111 1111
+FS -1 LSB	+VREF - 1LSB	0111 1111 1110
Midscale	0	0000 0000 0000
–FS +1 LSB	-VREF + 1LSB	1000 0000 0001
-FS	-VREF	1000 0000 0000

OUTPUT CODING : SINGLE-ENDED INPUT MODELS		
INPUT	VOLTAGE *(+INPUT) - (-INPUT)*	STRAIGHT BINARY CODING MSB LSB
+FS	+VREF	1111 1111 1111
+FS -1 LSB	+VREF - 1LSB	1111 1111 1110
Midscale	+VREF/2	1000 0000 0000
–FS +1 LSB	0V +1 LSB	0000 0000 0001
-FS	0V	0000 0000 0000

TECHNICAL NOTES

Reference Input

The full-scale range of the ADS-424/ADS-429 is set by the external low-noise reference voltage applied to the REF pin. The A/D will accept a reference voltage between +2.0V nominal to V_{DD}. Voltage applied to REF should not exceed V_{DD}. A decoupling capacitor of 0.1µF at the REF pin bypassed to GND is recommended.

Serial Digital Communication

The ADS-424 and ADS-429 employ an SPI compatible communication protocol for both reading and writing to the logic control section. The reading (SDO) and writing (SDI) functions are syncronizeed with a user provided SCLCK series of pulses applied during the conversion period of the data conversion process. Activity on the SCLCK should be done during the data transfer time (tdata) specified in the timing specifications and timing diagram. The internal configuation registers read and write data in an MSB to LSB format to control input channel selection as well as power saving configuration options. See the following Configuration Register Tables.

REGISTER CONFIGURATION

Bit 15 (MSB)	14	13	12	11	10	9	8
LD1	LD0	ADDR2	ADDR1	ADDR0	PS1	PS0	Not Used
Bit 7	6	5	4	3	2	1	Bit 0 LSB
RGRD	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

REGISTER DESCRIPTION

BIT(S)				
15:14	Set to "11" to load registers, else previous settings unchanged			
13:11	**Mux Channel Select**			
	ADDR2	**ADDR1**	**ADDR0**	**Channel**
	0	0	0	INPUT0 or +INPUT0/-INPUT0
	0	0	1	INPUT1 or +INPUT1/-INPUT1
	0	1	0	INPUT2 or +INPUT2/-INPUT2
	0	1	1	INPUT3 or +INPUT3/-INPUT3
	1	0	0	INPUT4
	1	0	1	INPUT5
	1	1	0	INPUT6
	1	1	1	INPUT7
10:9	**Power Saving Select**			
	PS1	**PS2**	Power Saving Mode	
	0	0	Power Down at end of next conversion 150µs recovery period	
	0	1	Fully powered at all times (default mode)	
	1	x	Sleep mode at end of next conversion 2.1µs recovery period	
8	Not Used			
7	Register readback: "1" sets register for configuration settings to be output with data out on SDO. "0" (default mode) configuration settings not exported.			
6:0	Not Used			

Power Saving Mode

These converters can be programmed through the input configuration register for one of two power saving modes of operation. Following the current conversion, the Power Down option shuts down all circuits with the exception of the internal oscillator and the digital interface. A recovery period of 150µs is required following the CONV asserted low.

The Sleep mode does not shut down as many circuits as the Power Down mode and therefore does not afford the same power-savings, however the recovery period for this mode of operation is only 2.1µs

Grounding and Layout

It is recommended that separate AGND and DGND ground planes be used. These two planes should be connected at the A/D however, the optimal connection location of the two planes may be system dependent. If separate DGND and AGND planes are used, all of the digital components and switching signals should be located over the DGND and all critical analog components and signals located over the AGND plane. In addition, a signal ground can be employed for all low current signal path grounding.

Power Supplies

To minimize power supply noise and maintain optimal SFDR and SNR performance, tantalum capacitors in parallel with 0.1uF capacitors should be placed as close as possible to the converter's power supply pins. Be assured that capacitors are bypassed to their proper AGND or DGND planes.

Humidity and Outgassing Susceptibility

Plastic mold compounds that are used to house ICs can absorb moisture. When these devices are exposed to humidity the plastic package can undergo slight changes that can apply pressure to the internal die. Stresses placed on a precision data converters can cause changes in its performance in the order of 100ppm. The fully hermetic package offered for the –QL and /883 versions are not affected by humidity, and are therefore more stable in environments where humidity is a concern. The –QL and /883 versions are recommended for all critical and High Reliability applications.

In addition to humidity concerns, the outgassing effects of plastic mold compounds that occur when exposed to temperature can have damaging effects on precision electronic circuits as well as releasing contaminants into purified environments. The hermetic properties of the ceramic LCC package offer protection not available with standard SMT packaging.

Board Mounting Considerations

For applications requiring the highest accuracy, attention should be paid to the board mounting location of SE and SM devices. These models use a plastic TSSOP package that could subject the die to mild stresses when the printed circuit board is cooled or heated. Placing the device in areas subject to slight twisting may cause die stresses and consequently degradation in the accuracy of the converter. It is preferred that the device be placed in the center of the PCB or near the edge of the shortest side where stresses due to flexing are reduced. Mounting the device in a cutout also minimizes flex. Mounting the device on an extremely thin PCB or flexprint will increase the potential for loss of accuracy due to stress. The CLCC package offered for -QL and /883 devices eliminates the potential for die stress.

Board Assembly Considerations

Precision converters provide high accuracy over temperature extremes, but some PC board assembly precautions are necessary. Changes in DC parameters can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

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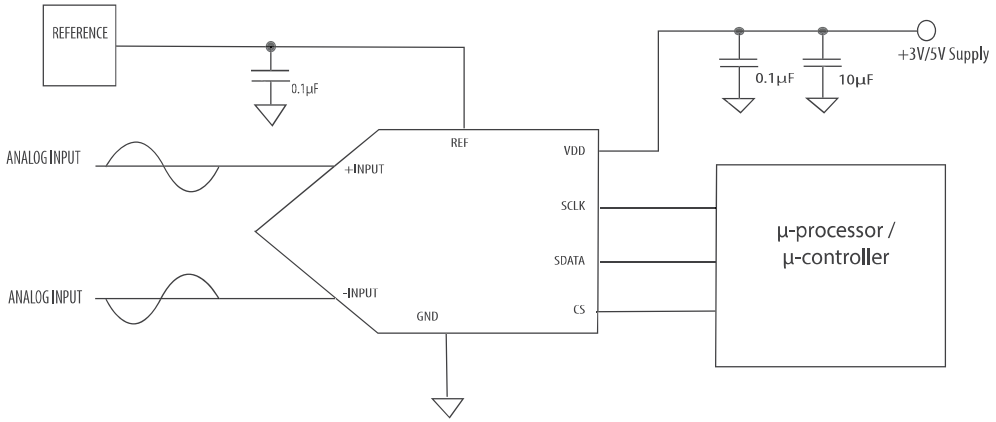
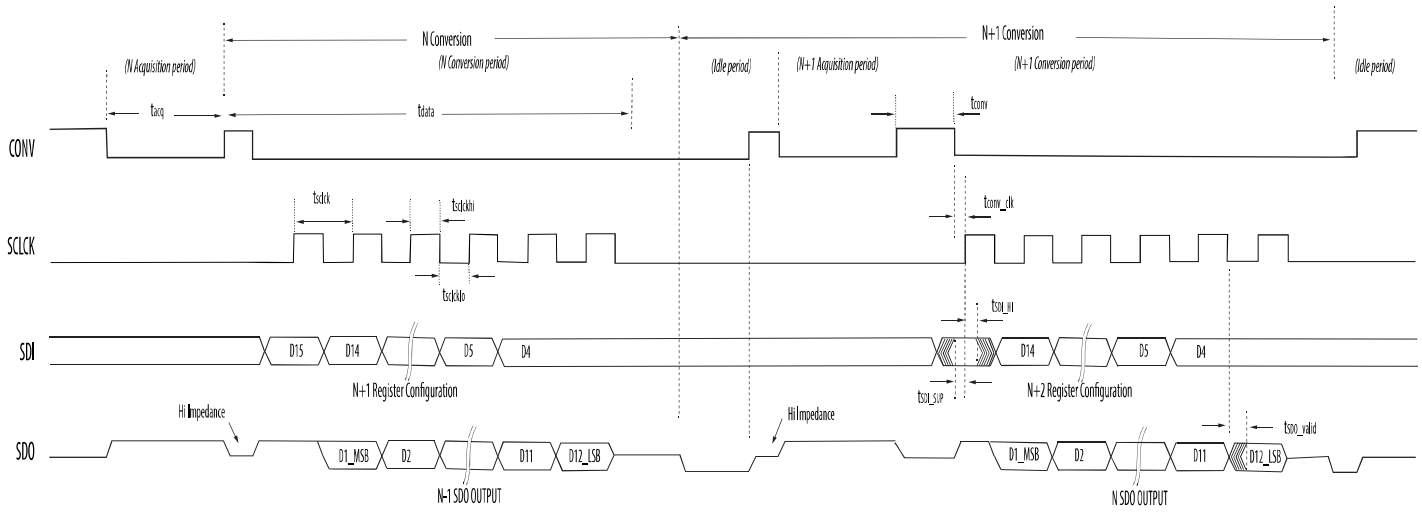
TYPICAL APPLICATION CONNECTION / PIN DESCRIPTIONS



Typical ADS-424/ADS-429 Connection Diagram

TIMING



ADS-424/ADS-429 Timing Diagram

GLOSSARY OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.
For +FS, This is the deviation of the last code transition (011...110 to 011...111) from the ideal (+INPUT) - (-INPUT) (i.e., +REF – 1 LSB), after the zero code error has been adjusted out.
For -FS, this is the deviation of the first code transition (100...000 to 100...001) from the ideal (+INPUT) - (-INPUT) (i.e., – REF + 1 LSB), after the zero code error has been adjusted out.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTERNAL REFERENCE VOLTAGE DRIFT: The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

OFFSET ERROR: The deviation from the ideal at analog zero output. This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal (+INPUT) - (-INPUT) (i.e., 0 LSB).

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

POWER SUPPLY REJECTION RATIO (PSRR): The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and Sample-Holds and D/A converters.

SPURIOUS FREE DYNAMIC RANGE (SFDR): The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

SIGNAL TO NOISE RATIO AND DISTORTION (SINAD): Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D including all the Harmonics.

SIGNAL TO NOISE RATIO (SNR): Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D excluding the first five Harmonics.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the Harmonics to the rms of the fundamental signal. It is usually expressed in dB.

TWO TONE INTERMODULATION DISTORTION: The change in a sinusoidal waveform that is caused by the presence of a second sinusoidal input of a different frequency. Typically specified in dB.

ACQUISITION TIME: For a sample-hold, the time required, after the sample command is given, for the hold capacitor to charge to a full scale voltage change and then remain within the specified error band of ±1/2 LSB.

APERTURE DELAY TIME: In a sample-hold, the time elapsed from the hold command to the actual opening of the sampling switch.

APERTURE JITTER: See Aperture uncertainty time

APERTURE TIME: The time window, or time uncertainty, in making a measurement. For an A/D converter the conversion time; for a sample- hold it is the signal averaging time during the sample to hold transition.

APERTURE UNCERTAINTY TIME: In a sample-hold, the time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample

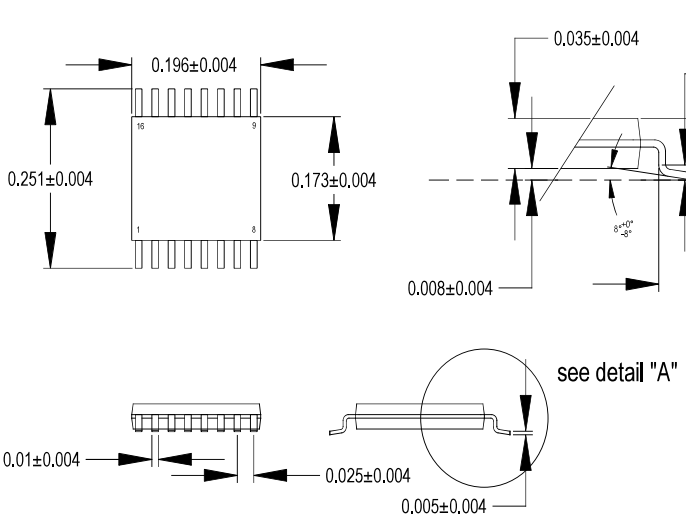
COMMON MODE REJECTION RATIO: is defined as the ratio of power of the A/D at FS max to the power of a 250mVpp sine wave applied to +INPUT and -INPUT, generally expressed in dB.

$$CMRR = 20 \log_{10} AD / ACM$$

where AD is the power of the A/D at FS and ACM is the power of the 250mVpp sine wave applied to +INPUT and -INPUT.

MECHANICAL DIMENSIONS – SURFACE MOUNT PACKAGE – INCHES (mm)

TSSOP



Dimensions are in Inches.
Dimensions do not include mold flash,
gate burrs, or protrusions.

ORDERING INFORMATION

ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE (°C)	PACKAGE	SHIPPING
ADS-424SE	-40 to +105	16 Pin TSSOP	Tube
ADS-424SM	-55 to +125	16 Pin TSSOP	Tube
ADS-424-QL	-55 to +125	Ceramic LCC	Tray
ADS-424/883	-55 to +125	Ceramic LCC	Tray
ADS-429SE	-40 to +105	16 Pin TSSOP	Tube
ADS-429SM	-55 to +125	16 Pin TSSOP	Tube
ADS-429-QL	-55 to +125	Ceramic LCC	Tray
ADS-429/883	-55 to +125	Ceramic LCC	Tray

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