ADSD-1410S

Dual 14-Bit, 10MSPS Sampling A/D Converter

FEATURES

- 14-bit resolution; 10MSPS sampling rate
- Functionally complete; ±2.5V input range
- No missing codes over full temperature range
- Edge-triggered
- ±5V supplies, 1.6 Watts
- 76dB SNR, –83dB THD
- Ideal for both time and frequency domain applications

PRODUCT OVERVIEW

The ADSD-1410S is a functionally complete, dual 14-bit, 10MSPS, sampling A/D converter. Its standard, 40-pin, triple-wide SMT DIP contains two fast-settling sample/hold amplifiers, two 14-bit A/D converters, multiplexed output buffers, a precision reference, and all the timing and control logic necessary to operate from either two or a single start convert pulse.

The ADSD-1410S is optimized for wideband frequency-domain applications and is fully FFT tested. The ADSD-1410S requires only ±5V supplies and typically consumes 1.6 Watts. The digital output power supply is capable of directly driving 5V or 3V logic systems. Models are available in either commercial 0 to +70°C or military -55 to +125°C operating temperature ranges.

FUNCTIONAL BLOCK DIAGRAM

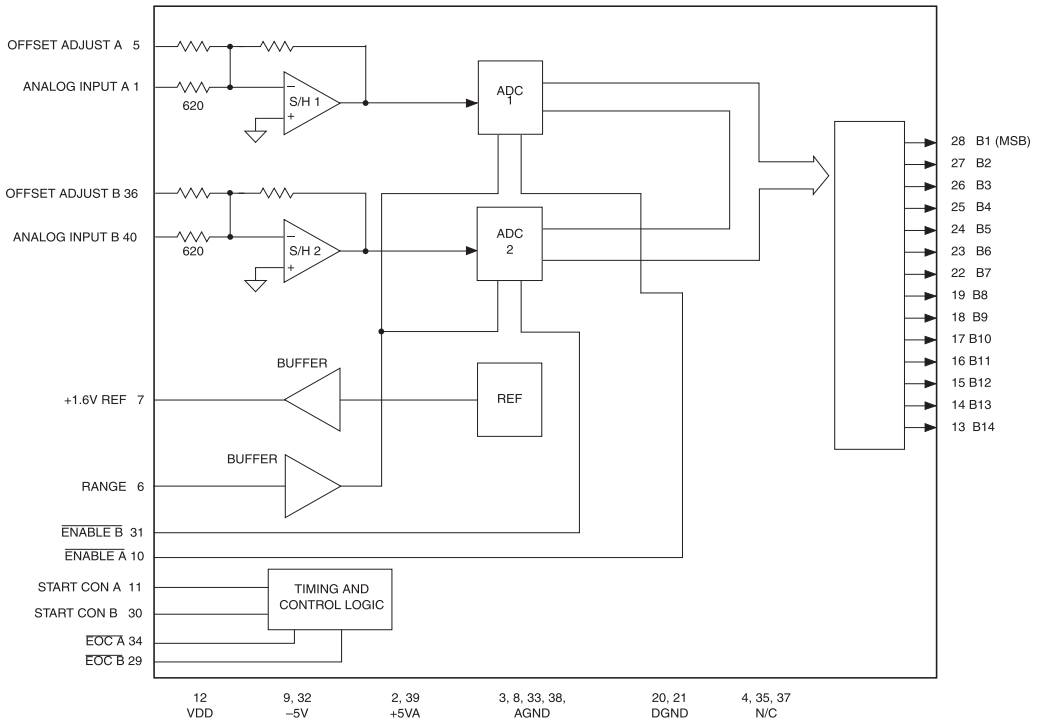


Figure 1. ADSD-1410S Functional Block Diagram

PARAMETERS	LIMITS	UNITS
+5VCC Supply (Pins 2, 39)	0 to +6	Volts
–5VEE Supply (Pins 9, 32)	0 to –6	Volts
VDD Supply (Pin 12)	–0.3 to (VCC +0.3)	Volts
Digital Inputs (Pins 10, 11, 30, 31)	–0.3 to (VDD +0.3)	Volts
Analog Input (Pins 1, 40)	±7	Volts
Lead Temp. (10 seconds)	+300	°C

FUNCTIONAL SPECIFICATIONS

(TA = +25°C, VCC = +5V, VDD = +5V, VEE = –5V, 10MSPS sampling rate,Vin = ±2.5V and a minimum 7 minute warmup unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	—	±2.5V	—	Volts
Input Impedence	610	620	630	Ω
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels	+2.4	—	—	Volts
Logic "1"	—	—	+0.8	Volts
Logic "0"	—	—	+10	µA
Logic Loading "1"	—	—	–10	µA
Logic Loading "0"				
PERFORMANCE				
Integral Non-Linearity				
+25°C (fin=10kHz)	—	±1	—	LSB
0 to +70°C	—	±1	—	LSB
–55 to +125°C	—	±2	—	LSB
Differential Non-Linearity				
(fin = 10kHz)				
+25°C	–0.99	±0.5	+1.5	LSB
0 to +70°C	–0.99	±0.5	+1.5	LSB
–55 to +125°C	–0.99	±0.75	+1.75	LSB
Offset Error				
+25°C (see Figure 3)	—	±0.25	±0.5	%FSR
0 to +70°C	—	±0.25	±0.5	%FSR
–55 to +125°C	—	±0.5	±0.8	%FSR
Gain Error				
+25°C (see Figure 3)	—	±0.3	±0.6	%FSR
0 to +70°C	—	±0.3	±0.6	%FSR
–55 to +125°C	—	±0.6	±0.8	%FSR
No Missing Codes	–55 to +125°C			
14 Bits				
Resolution	14 Bits			
OUTPUTS				
Output Coding	Offset Bin.			
Logic Level				
Logic "1" VDD = +5V	+3.8	—	—	Volts
VDD = +3.3V	+2.48	—	—	Volts
Logic "0" VDD = +5V	—	—	+0.5	Volts
VDD = +3.3V	—	—	+0.5	Volts
Logic Loading "1" VDD = +5V	—	—	–8	mA
VDD = +3.3V	—	—	–4	mA
Logic Loading "0" VDD = +5V	—	—	+8	mA
VDD = +3.3V	—	—	+4	mA
Internal Reference				
Voltage, +25°C	+1.5	+1.6	+1.7	Volts
0 to +70°C	+1.5	+1.6	+1.7	Volts
External Current	—	—	5	mA

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Total Harm. Distort. (–0.5dB)				
dc to 500kHz	—	–84	–80	dB
500kHz to 5MHz	—	–83	–75	dB
Signal-to-Noise Ratio				
(w/o distortion, –0.5dB				
dc to 500kHz	74	76	—	dB
500kHz to 5MHz	74	76	—	dB
Signal-to-Noise Ratio				
(and distortion, –0.5dB)				
dc to 500kHz	72	75	—	dB
500kHz to 5MHz	72	75	—	dB
Spurious Free Dyn. Range ①				
dc to 500kHz	—	–87	–82	dB
500kHz to 5MHz	—	–86	–78	dB
Two-tone IMD				
Distortion (fin = 4.85MHz,				
fs = 10MHz, –0.5dB)	—	–80	—	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	—	14	—	MHz
Large Signal (–0.5dB input)	—	14	—	MHz
Aperture Delay Time	—	—	±10	ns
Aperature Uncertainty	—	0.4	—	ps, RMS
S/H Acq. Time, (to ±0.003%FSR)				
Step input	—	—	25	ns
Feedthrough Rejection				
(fin = 5MHz)	—	85	—	dB
Noise	—	250	—	µVrms
TIMING SPECIFICATIONS				
Conversion Rate	1	—	10	MHz
Start Convert High	25	50	500	ns
Start Convert Low	25	50	500	ns
Start Convert to EOC				
EOC to Data Valid				
Output Disable Delay	1	6	13	ns
POWER REQUIREMENTS				
Power Supply Ranges				
–5VEE Supply	–5.25	–5.0	–4.75	Volts
+5VCC Supply	+4.75	+5.0	+5.25	Volts
VDD Supply	+3.0	+5.0	VCC	Volts
Power Supply Currents				
–5VEE Supply	–100	–89	—	mA
+5VCC Supply	—	+230	+245	mA
VDD Supply	—	+2.0	+5.0	mA
Power Dissipation	—	1.6	1.7	Watts
Power Supply Rejection	—	—	±0.02	%FSR%V
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, Ambient				
ADSD-1410S	0	—	+70	°C
ADSD-1410S-EX	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, SMT TDIP			

Footnote:

① Same specification as In-Band Harmonics and Peak Harmonics.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. Connect the digital and analog grounds to one point, the analog ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3. Apply a pulse of 50 nanoseconds typical to START CONVERT (pin 11) at a rate of 2MHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. **Zero (Offset) Adjustments**

   Apply a precision voltage reference source between ANALOG INPUT A (pin 1) and SIGNAL GROUND (pin 3), then adjust the reference source output per Table 2. Adjust trimpot R1 until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001.
3. Repeat above step for Analog Input B (Pin 40). Use trimpot R2 for the zero (Offset) adjustment .

Table 2. Offset Adjustment

INPUT RANGE	OFFSET ADJUST +1/2 LSB
±2.5V	+0.000153V

Table 3. Output Coding

OUTPUT CODING MSB LSB	INPUT RANGE ±2.5V	BIPOLAR SCALE
11 1111 1111 1111	+2.499695	+FS – 1LSB
11 1000 0000 0000	+1.875000	+3/4FS
11 0000 0000 0000	+1.250000	+1/2FS
10 0000 0000 0000	±0.000000	0
01 0000 0000 0000	–1.250000	–1/2FS
00 1000 0000 0000	–1.875000	–3/4FS
00 0000 0000 0001	–2.499695	–FS+1LSB
00 0000 0000 0000	–2.500000	–FS

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

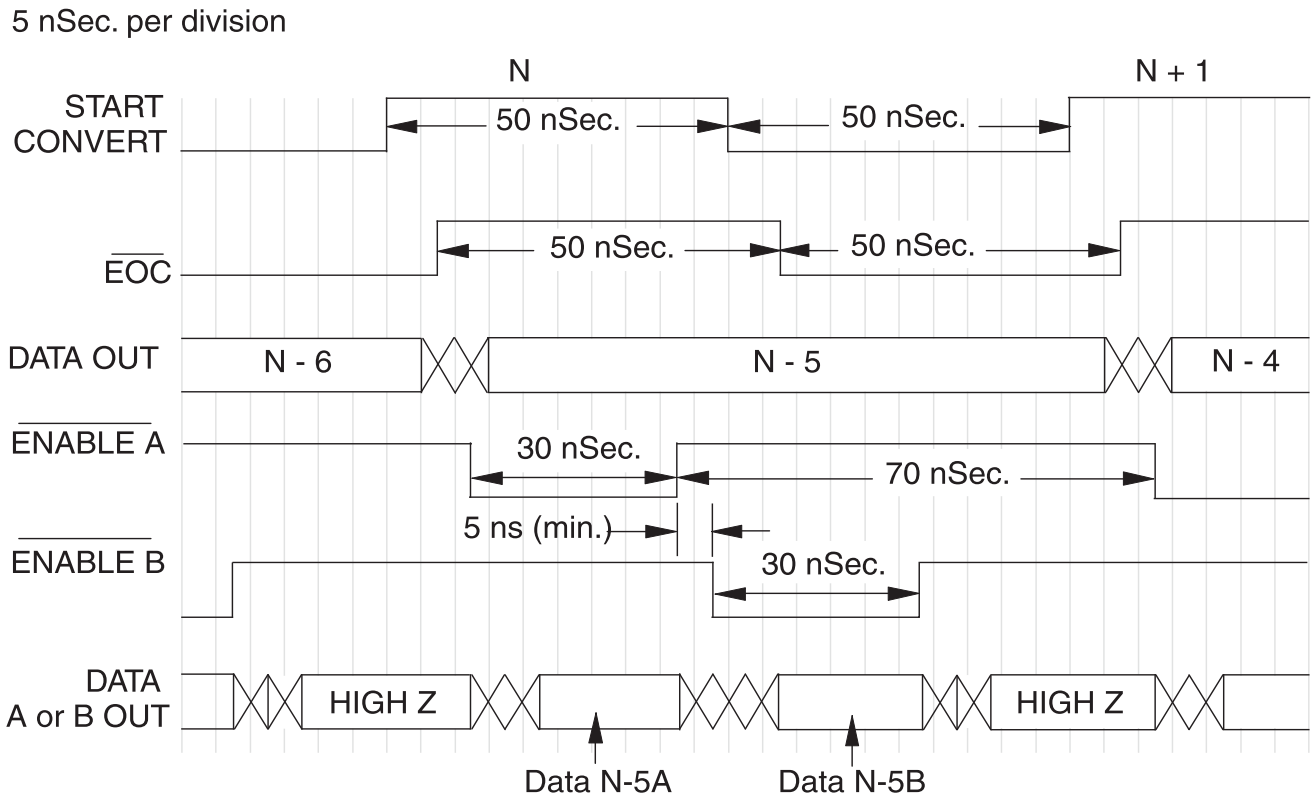
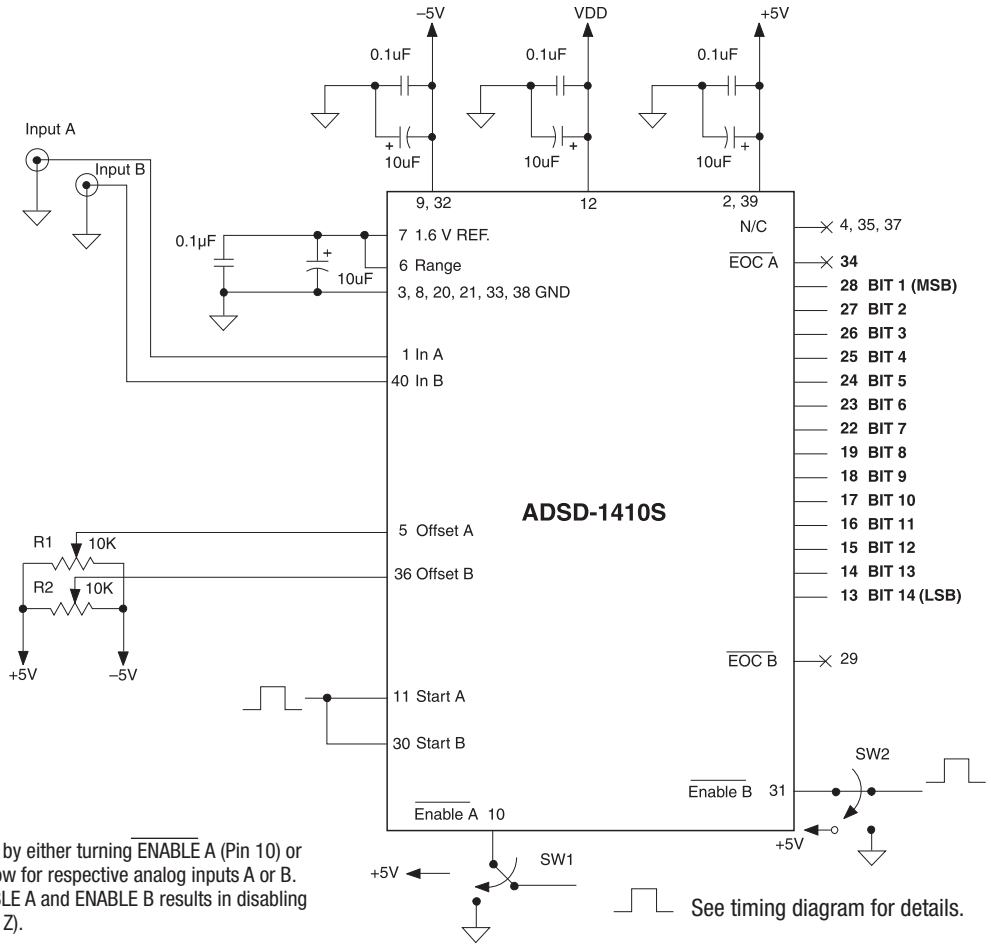


Figure 2. ADSD-1410S Timing Diagram



Notes:

① Outputs are enabled by either turning $\overline{\text{ENABLE}}$ A (Pin 10) or $\overline{\text{ENABLE}}$ B (Pin 31) low for respective analog inputs A or B. A high on both ENABLE A and ENABLE B results in disabling the output bus (High Z).

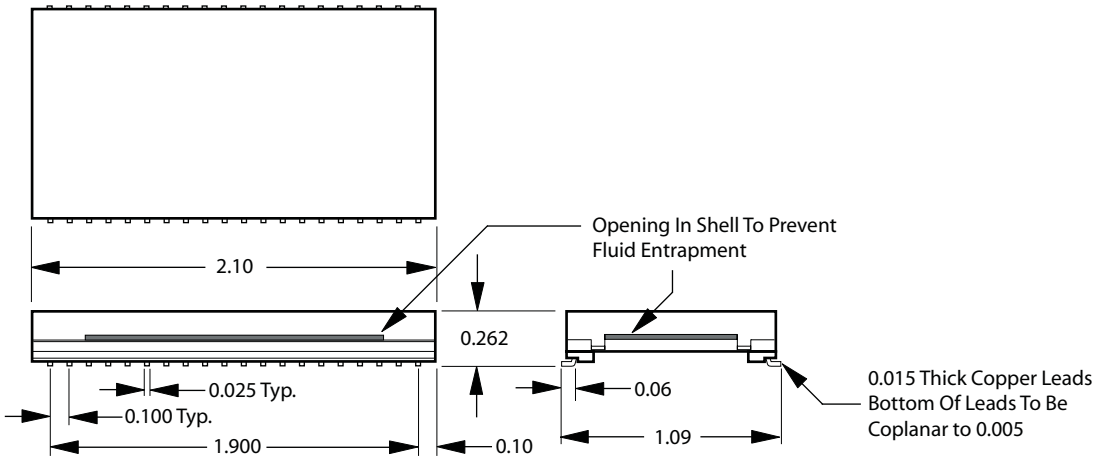
Figure 3. ADSD-1410S Connection Diagram

THERMAL REQUIREMENTS

The ADSD-1410S sampling A/D converter is fully characterized and specified over the commercial operating temperature (ambient) range of 0 to +70°C and military temperature range of –55 to +125°C (EX suffix). All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Minimal air flow over the surface can greatly help reduce the package temperature.

MECHANICAL DIMENSIONS INCHES (MM)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	PACKAGE	ROHS
ADSD-1410S	0 to +70°C	SMT-TDIP	No
ADSD-1410S-C	0 to +70°C	SMT-TDIP	Yes
ADSD-1410S-EX	-55to +125°C	SMT-TDIP	No
ADSD-1410S-EX-C	-55to +125°C	SMT-TDIP	Yes

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT A	40	INPUT B
2	+5VA	39	+5VA
3	ANALOG GROUND	38	ANALOG GROUND
4	N.C.	37	N.C.
5	OFFSET A	36	OFFSET B
6	RANGE	35	N.C.
7	1.6V REF	34	$\overline{\text{EOC A}}$
8	ANALOG GROUND	33	ANALOG GROUND
9	–5V	32	–5V
10	$\overline{\text{ENABLE A}}$	31	$\overline{\text{ENABLE B}}$
11	START A	30	START B
12	VDD	29	$\overline{\text{EOC B}}$
13	BIT 14 (LSB)	28	BIT 1 (MSB)
14	BIT 13	27	BIT 2
15	BIT 12	26	BIT 3
16	BIT 11	25	BIT 4
17	BIT 10	24	BIT 5
18	BIT 9	23	BIT 6
19	BIT 8	22	BIT 7
20	DGND	21	DGND