

**DAC-S** 



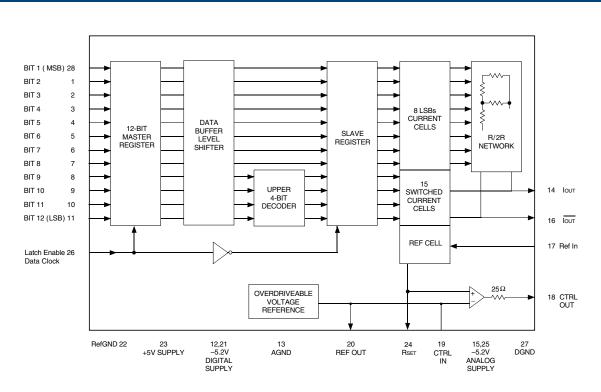
### **PRODUCT OVERVIEW**

The DAC-S is a 12-bit, ultra high speed, current output digital-to-analog converter. This TTL/CMOS compatible device converts at a rate of 100MHz and features a 3.0pV-s glitch energy and excellent frequency domain specifications.

The DAC-S develops complementary current outputs of 0 to -20.48mA and can directly drive 50 Ohm loads. The excellent dynamic specifications (to Nyquist at fOUT=2.02MHz) include an SFDR of -85dB. Static performance includes maximum over temperature specifications of  $\pm$ 1.75LSB and  $\pm$ 1.5LSB for integral and differential nonlinearity, respectively.

The DAC-S achieves low power and high speed performance from an advanced BiCMOS process. The architecture employs an R/2R resistor network and a segmented switching current cell arrangement to reduce glitch. Laser trimming assures that 12-bit linearity is achieved and maintained over the transfer curve. It also incorporates a 12-bit input data register and bandgap voltage reference with a buffer amplifier.

The DAC-S runs on +5V and -5.2V supplies and dissipates a maximum of 802mW. It is available in a 28-pin CLCC package with an operating temperature range of 0 to 70°C or -55 to +125°C.



### **FUNCTIONAL BLOCK DIAGRAM**

**FEATURES** 

100MHz conversion rate

Low power, 650mW, typical

Low glitch energy, 3.0pV-s

Excellent dynamic specifications

Pin compatible with Analog Devices AD9713

Models available in commercial (0 to + 70°C), indus-

trial (-40 to +100°C), or military (-55 to +125°C)

TTL/CMOS compatible inputs

operating temperature ranges

20ns settling time



ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
+5V Digital Supply	+5.5	Volts
-5.2V Digital Supply	-5.5	Volts
-5.2V Analog Supply	-5.5	Volts
Digital Input Voltages	-0.5 to +5V Supply level	Volts
Internal Reference Output Current	±2.5	mA
Voltage from CTRL IN to -5.2V (A) Supply	2.5 to 0	Volts
CTRL OUT Output Current	±2.5	mA
Reference Input Voltage Range	-5.2V (A) Supply Level to -3.7	Volts
Analog Output Current, IOUT	30	mA
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temperature Range	·			
DAC-S/MC & -C	0	_	+70	°C
DAC-S/ME & -C	-40		+100	°C
DAC-S & -C	-55	_	+125	°C
Storage Temperature Range	-65	_	+150	°C
Thermal Resistance, θja		24		(°C/W)
Junction Temperature	_		+150	°C
Package Type	28 Pin CLCC			

## **FUNCTIONAL SPECIFICATIONS**

(TA = See specification table, -5.2V (A) Supply = -5.2V (D) Supply = -4.94 to -5.46V, +5V Supply = 4.75 to 5.25V, VREF = Internal, RL = 50 Ohms and fs = 100MHz unless otherwise specified.)

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			0 TO +70°C			–55 T0 +125°C		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	DIGITAL INPUTS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		12	—	—	12	_	—	Bits
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		+2.0		_	+2.0		_	Volts
Logic Loading "1"           400           400 $\mu$ A           Logic Loading "0"           700           700 $\mu$ A           Digital input Capacitance, CIN          3.0         15          3.0         15         pF           TMING CHARACTERISTICS           3.0         2          ns           Data setup fine, Isu         0.5         0.25          ns         ns         ns           Propagation Delay Time, Isu         0.5         0.25          ns         ns         ns           STATIC PERFORMANCE          -         3           ns         statistic field		+2.0	_		+2.0	_		
Logic Loading "0"         —         —         700         —         —         700         µA           Digital Input Capacitance, CIN         —         3.0         15         —         3.0         15         pF           Data setup time, tsu         3         2         —         3.0         2         —         ns           Data setup time, tsu         3         2         —         0.5         0.25         —         ns           Propagation Delay Time, tsu         —         —         4.5         7         —         4.5         7         ns           CLOCK Puise Width, Ten V.         —         4.5.         7         —         4.5         7         ns           STATIC PERFORMANCE         —         ±0.75         ±1.0         —         ±1.75         LSB           Offset Error         —         20         75         —         0.5         ±1         LSB           Output Votage Setting Time, tSET         —         10         —         2         10         PV-s           Full Scale Step to ±0.5LSB         —         20         22         —         20         22         ns           Glitch Area         …         11 </td <td></td> <td>_</td> <td></td> <td></td> <td>_</td> <td>_</td> <td></td> <td></td>		_			_	_		
Digital Input Capacitance, CIN		_				_		
Data setup time, tsu         3         2          3         2          ns           Data setup time, tsu         0.5         0.25          0.5         0.25          ns           Propagation Delay Time, tsu           3           ns           STATE PERFORMANCE           3           ns           STATE PERFORMANCE           3           ns           STATE PERFORMANCE           20         75          20         75         µA           Gain Error @           100           MHz           Oversion Rate @         100           100           MHz           Output Voltage Setting Time, ISET          11         13          12         15         ns           Full Scale Step to ±1LSB          11         13          12         15         ns           Singlet (Peak)          2         10	Digital Input Capacitance, CIN	—	3.0	15	_	3.0	15	
Data Hold Time, Ison         0.5         0.25          0.5         0.25          ns           Propagation Delay Time, Ison          4.5         7         ns         ns           CLOCK Pulse Width, Tsw1, Tsw2         3           3          ns           STATIC PERFORMANCE          ±0.75         ±1.0          ±1.0         ±1.75         LSB           Differential Nonlinearity          ±0.5         ±.75          0.5         ±1         LSB           Offset Error          20         75          0.5         ±1         LSB           Offset Error          ±1         ±10          ±1         ±10         %           DYNAMIC PERFORMANCE           100          ±1         ±10         %           Conversion Rate ③         100          20         22         ns         s         ns         Full Scale Step to ±0.5LSB         ns         s         pV-s           Singlet (Peak)          2         10          2         10         pV-s	TIMING CHARACTERISTICS							
Propagation Delay Time, too          4.5         7          4.5         7         ns           STATIC PERFORMANCE           Integral Nonlinearity          ±0.75         ±1.0          ±1.0         ±1.75         LSB           Differential Nonlinearity          ±0.5         ±7.5          0.5         ±1         LSB           Offset Error          20         75          20         75         µA           Gain Error ©          ±1         ±10          ±1         ±10         %           PYNAMIC PERFORMANCE           Conversion Rate ③         100           100           101         %           PYNAMIC PERFORMANCE           Error ③         100          11         13          12         15         ns           Full Scale Step to ±1.58          21         10          2         10         PV-s           State Step to ±0.51.58          2         10         PV-s         0utp							—	
CLÓCK Pulse Width, Twi, Twi2         3           3           ns           STATIC PERFORMANCE           Integral Nonlinearity ①          ±0.75         ±1.0         ±1.75         LSB           Offset Error          20         75          0.5         ±1         LSB           Offset Error          ±1         ±10         -         ±1         ±10         %           Offset Error          11         13          12         15         ns           Conversion Rate @         100          20         22         ns         16           Full Scale Step to ±1LSB          11         13          12         15         ns <td></td> <td>0.5</td> <td></td> <td></td> <td>0.5</td> <td></td> <td></td> <td></td>		0.5			0.5			
STATIC PERFORMANCE           Integral Nonlinearity         - $\pm 0.75$ $\pm 1.0$ - $\pm 1.75$ LSB           Differential Nonlinearity         - $\pm 0.5$ $\pm 75$ - $0.5$ $\pm 1$ LSB           Offset Error         - $20$ $75$ - $20$ $75$ $\mu A$ Gain Error @         - $\pm 1$ $\pm 10$ - $\pm 1$ $\pm 10$ %           DVNAMIC PERFORMANCE           Conversion Rate @         100         -         MHz           Output Voltage Setting Time, tSET         -         11         13         -         12         15         ns           Full Scale Step to $\pm 1LSB$ -         11         13         -         12         15         ns           Glitch Area         -         20         22         -         20         22         ns         90           Singlet (Peak)         -         3         -         200         00         pV-s         0utput Site Time         900         1000         -         900         1000         W/us								
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		3	—	—	3	_	—	ns
Differential Nonlinearity          ±0.5         ±.75          0.5         ±1         LSB           Offset Error          20         75          20         75         µA           Gain Error ②          ±1         ±10          ±1         ±10         %           PVNAMC PERFORMANCE          11         13          12         15         ns           Conversion Rate ③         100           100           MHz           Output Voltage Setting Time, tSET          11         13          12         15         ns           Full Scale Step to ±0.5LSB          20         22          20         22         ns           Glitch Area          2         10          2         10         pV-s           Doublet (Net)          3           3          pV-s           Output Siew Rate         900         1000          900         1000          ps           Differential Cain <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>								
Offset Error         −         20         75         −         20         75         µA           Gain Error ②         −         ±1         ±10         −         ±1         ±10         %           DYNAMIC PERFORMANCE                %           Conversion Rate ③         100         −         −         100         −         −         MHz           Output Voltage Setting Time, tSET         −         11         13         −         12         15         ns           Full Scale Step to ±0.5LSB         −         20         22         −         20         22         ns           Glitch Area         −         2         10         −         2         10         pV-s           Doublet (Net)         −         3         −         −         3         −         pV-s           Output Slew Rate         900         1000         −         900         1000         −         ps           Differential Gain         −         0.15         −         −         0.15         −         ps           Differential Gain         −         0.07         − <td></td> <td>—</td> <td></td> <td></td> <td>—</td> <td></td> <td></td> <td></td>		—			—			
Gain Error (2)        ±1       ±10        ±1       ±10       %         DYNAMIC PERFORMANCE         Conversion Rate (3)       100         100         MHz         Output Voltage Settling Time, ISET        11       13        12       15       ns         Full Scale Step to ±0.5LSB        20       22        20       22       ns         Gitch Area        2       10        2       10       pV-s         Singlet (Peak)        2       10        2       10       pV-s         Doublet (Net)        3         3        pV-s         Output Siew Rate       900       1000        900       1000        V/us         Output Siew Rate       900       1000        425       675        ps         Output Fall Time       425       470        425       470        ps         Differential Gain        0.07        0.07        p		—			—			
DYNAMIC PERFORMANCE           Conversion Rate ③         100         -         -         100         -         -         MHz           Output Voltage Settling Time, tSET         -         11         13         -         12         15         ns           Full Scale Step to ±0.5LSB         -         20         22         -         20         22         ns           Glitch Area         -         2         10         -         2         10         pV-s           Doublet (Net)         -         3         -         -         3         -         pV-s           Output Stew Rate         900         1000         -         900         1000         -         V/us           Output Stew Rate         900         1000         -         900         1000         -         V/us           Output Stew Rate         900         1000         -         900         1000         -         V/us           Output Stew Rate         900         1000         -         0.015         -         ps           Output Stew Rate         900         0.07         -         0.15         -         %         Mitz           Differential Phase <td></td> <td>—</td> <td></td> <td></td> <td>—</td> <td></td> <td></td> <td>μΑ</td>		—			—			μΑ
Conversion Rate ③         100           100           MHz           Output Voltage Settling Time, tSET          11         13          12         15         ns           Full Scale Step to ±0.5LSB          20         22          20         22         ns           Glitch Area          2         10          2         10         pV-s           Doublet (Net)          3           3          pV-s           Output Siew Rate         900         1000          900         1000          V/s           Output Siew Rate         900         1000          900         1000          V/s           Output Siew Rate         900         1000          900         1000          V/s           Output Siew Rate         900         1000          425         675          ps           Differential Gain          0.15          0.07          0.07          Deg           Spurious Free D		_	±1	±10	—	±1	±10	%
Output Voltage Settling Time, tSET         -         11         13         -         12         15         ns           Full Scale Step to ±0.5LSB         -         20         22         -         20         22         ns           Singlet (Peak)         -         2         10         -         2         10         pV-s           Doublet (Net)         -         3         -         -         3         -         py-s           Output Slew Rate         900         1000         -         900         1000         -         ps           Output Slew Rate         900         1000         -         900         1000         -         ps           Output Slew Rate         900         1000         -         900         1000         -         ps           Output Slew Tate         900         1000         -         425         675         -         ps           Output FilesTime         625         675         -         0.07         -         0.07         -         peg           Differential Phase         -         0.07         -         0.07         -         Deg         -         fCLK=10MSPS, f0UT=1.23MHz         -								
Full Scale Step to ±1LSB        11       13        12       15       ns         Full Scale Step to ±0.5LSB        20       22        20       22       ns         Glitch Area         2       10        2       10       pV-s         Doublet (Net)        3         3        pV-s         Output Siew Rate       900       1000        900       1000        V/µs         Output Rise Time       625       675        625       675        ps         Differential Gain        0.15         0.07        ps         Differential Phase        0.07        0.07        ps         Spurious Free Dynamic Range, Srom          77       dB         fCLK=20MSPS, f0UT=1.23MHz          77       dB         fCLK=20MSPS, f0UT=10.1MHz          75       71       dB         fCLK=40MSPS, f0UT=10.1MHz		100			100	—	—	MHz
Full Scale Step to ±0.5LSB        20       22        20       22       ns         Glitch Area        2       10        2       10       pV-s         Doublet (Net)        3         3        pV-s         Output Slew Rate       900       1000        900       1000        V/µs         Output Slew Rate       900       1000        900       1000        PV-s         Output Slew Rate       900       1000        900       1000        PV-s         Output Slew Rate       900       1000        900       1000        PV-s         Output Slew Rate       900       1000        900       1000        Py-s         Output Slew Rate       000       10.5         0.15        Ps         Differential Phase        0.07        0.07        Deg         Spurious Free Dynamic Range, Srow         77       dB       CLK=10MSPS, fOUT=1.23MHz				10		10		
Glitch Area         Singlet (Peak)       -       2       10       -       2       10       pV-s         Doublet (Net)       -       3       -       -       3       -       pV-s         Output Slew Rate       900       1000       -       900       1000       -       V/us         Output Rise Time       625       675       -       625       675       -       ps         Output Fail Time       425       470       -       425       470       -       ps         Differential Gain       -       0.15       -       -       0.07       -       Deg         Spurious Free Dynamic Range, Sepa       -       0.07       -       -       82       77       dB         fCLK=10MSPS, fOUT=1.23MHz       -       -       -       77       74       dB         fCLK=20MSPS, fOUT=5.05SMHz       -       -       -       75       71       dB         fCLK=20MSPS, fOUT=10.1MHz       -       -       -       78       75       dB         fCLK=80MSPS, fOUT=5.1MHz       -       -       -       79       75       dB         fCLK=100MSPS, fOUT=10.1MHz       -		_						
Singlet (Peak)        2       10        2       10       pV-s         Doublet (Net)        3         3        pV-s         Output Slew Rate       900       1000        900       1000        V/µs         Output Rise Time       625       675        625       675        ps         Output Fall Time       425       470        425       470        ps         Differential Gain        0.15        0.07        Deg         Spurious Free Dynamic Range, Sron          77       74       dB         fCLK=20MSPS, fOUT=1.23MHz          75       71       dB         fCLK=20MSPS, fOUT=16.MHz          75       71       dB         fCLK=30MSPS, fOUT=10.1MHz          78       75       dB         fCLK=50MSPS, fOUT=10.1MHz          79       75       dB         fCLK=100MSPS, fOUT=5.1MHz          79		_	20	22		20	22	ns
Doublet (Net)          3           3          pV-s           Output Slew Rate         900         1000          900         1000          V/µs           Output Rise Time         625         675          625         675          ps           Output Fall Time         425         470          425         470          ps           Differential Gain          0.15           0.07          Deg           Spurious Free Dynamic Range, Srow          0.07          0.07          Deg           fCLK=10MSPS, f0UT=1.23MHz            0.07          Deg           spurious Free Dynamic Range, Srow            82         77         dB           fCLK=20MSPS, f0UT=1.23MHz            75         71         dB           fCLK=20MSPS, fOUT=5.055MHz            77         74         dB           fCLK=40MSPS, f0UT=10.1MHz            7			0	10		0	10	2/10
Output Slew Rate         900         1000          900         1000          V/µs           Output Rise Time         625         675          625         675          ps           Output Fall Time         425         470          425         470          ps           Differential Gain          0.15           0.15          %           Differential Phase          0.07           0.07          Deg           Spurious Free Dynamic Range, SFDR           0.07          Deg            Spurious Free Dynamic Range, SFDR            0.07          Deg           Spurious Free Dynamic Range, SFDR            0.07          Deg           fCLK=10MSPS, fOUT=1.23MHz            77         74         dB           fCLK=20MSPS, fOUT=5.055MHz            75         71         dB           fCLK=50MSPS, foUT=10.1MHz </td <td></td> <td></td> <td></td> <td>10</td> <td></td> <td></td> <td>10</td> <td></td>				10			10	
Output Rise Time         625         675          625         675          ps           Output Fall Time         425         470          425         470          ps           Differential Gain          0.15           0.15          %           Differential Phase          0.07           0.07          Deg           Spurious Free Dynamic Range, SFDR            0.07          Deg           fCLK=10MSPS, f0UT=1.23MHz            82         77         dB           fCLK=20MSPS, foUT=5.055MHz            75         71         dB           fCLK=20MSPS, f0UT=16 MHz            75         71         dB           fCLK=50MSPS, f0UT=10.1MHz            78         75         dB           fCLK=100MSPS, f0UT=10.1MHz            79         75         dB           Throughput rate         100           79         75					000		_	
Output Fall Time         425         470          425         470          ps           Differential Gain          0.15          0.15          %           Differential Phase          0.07           0.07          Deg           Spurious Free Dynamic Range, SFDR            0.07          Deg           fCLK=10MSPS, f0UT=1.23MHz             82         77         dB           fCLK=20MSPS, f0UT=5.055MHz            75         71         dB           fCLK=40MSPS, f0UT=16 MHz            75         71         dB           fCLK=50MSPS, f0UT=10.1MHz            75         71         dB           fCLK=50MSPS, f0UT= 5.1MHz            78         75         dB           fCLK=100MSPS, f0UT=10.1MHz            79         75         dB           fCLK=100MSPS, f0UT=10.1MHz            79         75 <td< td=""><td></td><td></td><td></td><td>_</td><td></td><td></td><td>_</td><td></td></td<>				_			_	
Differential Gain        0.15        0.15        %         Differential Phase        0.07         0.07        Deg         Spurious Free Dynamic Range, SrDR          0.07        Deg         fCLK=10MSPS, f0UT=1.23MHz          82       77       dB         fCLK=20MSPS, f0UT=5.055MHz          77       74       dB         fCLK=20MSPS, f0UT=10.1MHz          75       71       dB         fCLK=50MSPS, f0UT=10.1MHz          78       75       dB         fCLK=80MSPS, f0UT=10.1MHz          78       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         fThroughput rate       100         79       75       dB         MALOG OUTPUT         100         MSPS				_			_	
Differential Phase       -       0.07       -       -       0.07       -       Deg         Spurious Free Dynamic Range, SFDR       -       -       -       -       82       77       dB         fCLK=20MSPS, f0UT=1.23MHz       -       -       -       -       82       77       dB         fCLK=20MSPS, f0UT=5.055MHz       -       -       -       -       77       74       dB         fCLK=40MSPS, f0UT=10.1MHz       -       -       -       75       71       dB         fCLK=50MSPS, f0UT=10.1MHz       -       -       -       78       75       dB         fCLK=80MSPS, f0UT=10.1MHz       -       -       -       78       75       dB         fCLK=100MSPS, f0UT=10.1MHz       -       -       -       79       75       dB         fCLK=100MSPS, f0UT=10.1MHz       -       -       -       79       75       dB         fCLK=100MSPS, f0UT=10.1MHz       -       -       -       79       75       dB         fThroughput rate       100       -       -       100       -       MSPS         ANALOG OUTPUT       -       -       -       -       -       20.48							_	
Spurious Free Dynamic Range, SFDR         fCLK=10MSPS, fOUT=1.23MHz         82       77       dB         fCLK=20MSPS, fOUT=5.055MHz          77       74       dB         fCLK=40MSPS, fOUT=16 MHz          77       74       dB         fCLK=40MSPS, fOUT=10.1MHz          75       71       dB         fCLK=50MSPS, fOUT= 10.1MHz          80       76       dB         fCLK=80MSPS, fOUT= 10.1MHz          78       75       dB         fCLK=100MSPS, fOUT=10.1MHz          78       75       dB         fCLK=100MSPS, fOUT=10.1MHz          79       75       dB         Throughput rate       100         700        MSPS         ANALOG OUTPUT        -20.48        -20.48        mA		_					_	
fCLK=10MSPS, fOUT=1.23MHz          82       77       dB         fCLK=20MSPS, fOUT=5.055MHz          77       74       dB         fCLK=40MSPS, fOUT=16 MHz          77       74       dB         fCLK=40MSPS, fOUT=10.1MHz          75       71       dB         fCLK=50MSPS, fOUT= 10.1MHz          80       76       dB         fCLK=80MSPS, fOUT= 10.1MHz          78       75       dB         fCLK=100MSPS, fOUT=10.1MHz          79       75       dB         fCLK=100MSPS, fOUT=10.1MHz          79       75       dB         Throughput rate       100         100        MSPS         ANALOG OUTPUT        -20.48         -20.48        mA			0.07			0.07		Dog
fCLK=20MSPS, f0UT=5.055MHz          77       74       dB         fCLK=40MSPS, f0UT=16 MHz         75       71       dB         fCLK=50MSPS, f0UT=10.1MHz         76       76       dB         fCLK=80MSPS, f0UT=5.1MHz          78       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         Throughput rate       100         100        MSPS         ANALOG OUTPUT        -20.48        -20.48        mA		_	_	_	_	82	77	dB
fCLK=40MSPS, fOUT=16 MHz         75       71       dB         fCLK=50MSPS, fOUT= 10.1MHz         80       76       dB         fCLK=80MSPS, fOUT= 5.1MHz         78       75       dB         fCLK=100MSPS, fOUT=10.1MHz         79       75       dB         fCLK=100MSPS, fOUT=10.1MHz         79       75       dB         Throughput rate       100         100        MSPS         ANALOG OUTPUT        -20.48        -20.48        mA		_		_	_			
fCLK=50MSPS, f0UT= 10.1MHz          80       76       dB         fCLK=80MSPS, f0UT= 5.1MHz          78       75       dB         fCLK=100MSPS, f0UT=10.1MHz          79       75       dB         Throughput rate       100         100        MSPS         ANALOG OUTPUT        -20.48        -20.48        mA		_			_			
fCLK=80MSPS, f0UT= 5.1MHz       —       —       —       78       75       dB         fCLK=100MSPS, f0UT=10.1MHz       —       —       —       79       75       dB         Throughput rate       100       —       —       100       —       MSPS         ANALOG OUTPUT       Full Scale Output Current       —       -20.48       —       —       -20.48       —       mA		_			_			
fCLK=100MSPS, f0UT=10.1MHz       —       —       —       79       75       dB         Throughput rate       100       —       —       100       —       MSPS         ANALOG OUTPUT		_						
Throughput rate         100         —         100         —         MSPS           ANALOG OUTPUT		_	_	_	_			
ANALOĞ OUTPUT Full Scale Output Current — –20.48 — — –20.48 — mA		100	_	_	100	_	_	MSPS
Output Voltage Compliance ④         -1.25          0         -1.25          0         Volts	Full Scale Output Current	_	-20.48	_	_	-20.48	_	mA
	Output Voltage Compliance ④	-1.25		0	-1.25	—	0	Volts



		0 T0 +70°C		-	-55 T0 +125°C		
INTERNAL REFERENCE/AMPLIFIER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Reference Voltage, VREF	-1.27	-1.23	-1.17	-1.27	-1.23	-1.17	Volts
Reference Voltage Drift	—	50	100	—	175	100	µV/°C
Reference Current Sink/Source Capability Reference Load Regulation	-125		+50	-125	—	+50	μA
$(IREF = 0 \text{ to } -125\mu \text{A})$	_	50	_	_	50	_	μV
Reference Input (CTRL IN) Impedance	_	12	_	10	12	_	kOhms
Reference Input (CTRL IN) Multiplying Bandwidth							
(100mV sine wave, to -3dB loss at IOUT)	50	200	_	50	200	_	MHz
Input Impedance at REF OUT	3	1.4	_	3	1.4	_	kOhms
Amplifier Large Signal Bandwidth							
(4V p-p sine wave input, to slew rate limit)	1	3	_	1	3	_	MHz
Amplifier Small Signal Bandwidth							
(1V p-p sine wave input, to –3dB loss)	4	10	—	4	10	_	MHz
POWER REQUIREMENTS							
Power Supply Ranges							
+5V Supply	+4.75	_	+5.25	+4.75		+5.25	Volts
-5.2V Supplies	-4.94	—	-5.46	-4.94	—	-5.46	Volts
Power Supply Currents							
+5V Supply	_	13	20	_	13	20	mA
-5.2V Digital Supply	_	70	85	_	70	95	mA
-5.2V Analog Supply	—	42	50	_	42	50	mA
Power Dissipation	—	650	800	_	650	800	mW
Power Supply Rejection (±5% variation)	_	5	10		5	10	μA/V

Footnotes:

① Best fit straight line.

② Gain Error measured as the error in the ratio between the full scale output current and the current through RsET (1.28mA typ.). Ideally the ratio should be 16.

③ Clock frequency range is from DC to the guaranteed minimum conversion rate.

④ Dynamic Range must be limited to a 1V swing within the compliance range.

# **TECHNICAL NOTES**

### **Clock Termination**

The internal 12-bit register is updated on the rising edge of the Latch Enable (pin 26). To minimize reflections and noise at high clock speeds proper termination techniques should be used. In the PCB layout the clock runs should be kept as short as possible and have minimal loading. The PCB should employ a controlled characteristic line impedance (Z<sub>0</sub>) of 50 Ohms. A shunt termination resistor, equal to Z<sub>0</sub>, should be placed as close to the CLOCK pin as possible, see Figure 2. The rise, fall and propagation delay times will be effected by the shunt termination resistor.

### **Digital Inputs**

The DAC-S is TTL/CMOS compatible. Data is latched by a Master register.

### **Outputs**

The outputs lout (pin 14) and  $\overline{lout}$  (pin 16) are complementary current outputs. Current is steered to either lout or  $\overline{lout}$  in proportion to the input code.

The sum of the two currents is always equal to the full scale current minus one LSB. See Table 1. The output can be converted to a voltage through a load resistor, typically 50 Ohms. Both current outputs should have the same load resistance value. See Figure 2. The output voltage generated is:

VOUT = IOUT (ROUT || 227 Ohms)

where 227 Ohms is the nominal DAC output resistance.

#### Table 1. Input Coding Table

INPUT CODE						
MSB	LSB	lout (mA)	lout (mA)			
1111 111	1 1111	-20.48	0			
1000 000	0000 00	-10.24	-10.24			
0000 000	0000 00	0	-20.48			



# **POWER SUPPLIES**

In order to reduce power supply noise separate -5.2V analog and digital power supplies should be used. The power supply lines should be bypassed with  $0.1\mu$ F and  $0.01\mu$ F ceramic capacitors placed as close to the -5.2V analog pins (15, 25) and digital pins (12, 21) as possible. The analog and digital power supply ground returns should be connected at one point as close to the power source as possible. The +5V supply pin (23) should be bypassed with a  $0.1\mu$ F ceramic capacitor connected as close to the pin as possible. See Figure 2.

## REFERENCE

The internal reference is a -1.23V, typical, bandgap voltage reference. The internal reference is connected to Reference OUT (REF OUT, pin 20) and the internal control Amplifier (CTRL IN, pin 19). The control Amplifier OUT (CTRL OUT, pin 18) should be connected to Reference IN (REF IN, pin17) and to -5.2V (pin 15) Analog Supply through a  $0.1\mu$ F ceramic capacitor (as shown in figure 2) in order to improve the settling time This reduces switching noise and improves output settling time. The Full Scale Output Current, Iour (pin 14) and Iour (pin 16), is controlled by the REF OUT (pin 20) voltage and the REF (pin 24) resistor through the following equation:

Full Scale Iout = [REF OUT Voltage/(Rset Resistance + 100Ω)] x 16

Note: Internal  $100\Omega$  is  $\pm 1\%$  tolerance

The internal reference (REF OUT) may be overdriven with a more precise external reference, capable of delivering up to 2mA, to provide better over temperature performance.

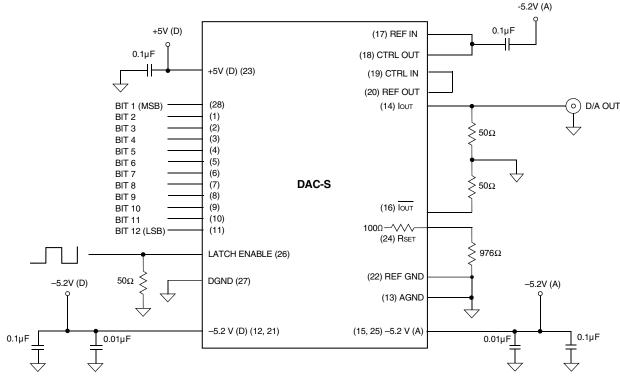
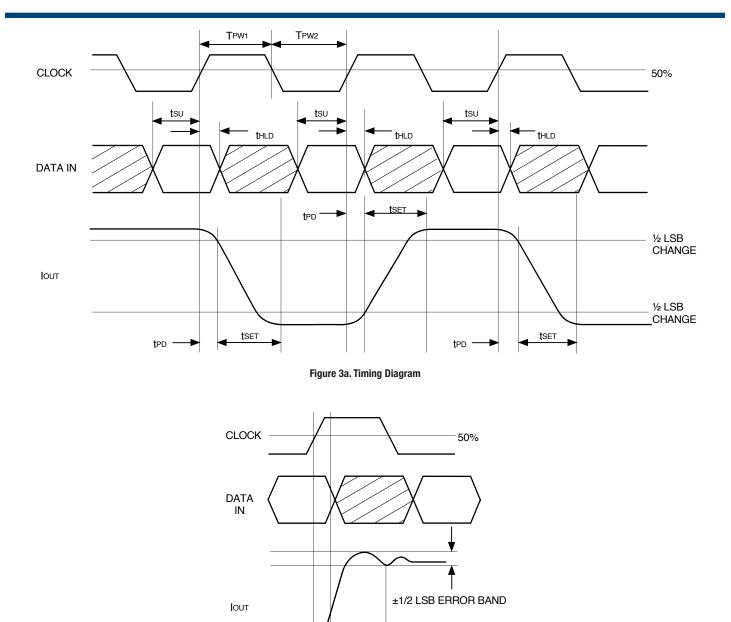


Figure 2. Typical Connection Diagram



DAC-S



tPD

**t**SET

Figure 3b. Full Scale Settling Time Diagram



DAC-S

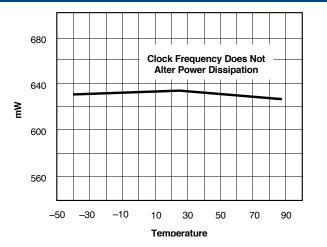
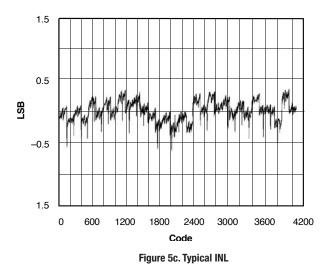


Figure 5a. Typical Power Dissipation Over Temperature



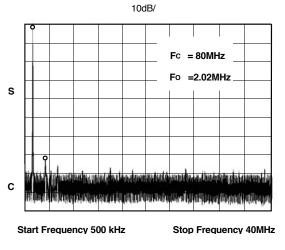


Figure 5e. Spurious Free Dynamic Range = 70.5dB

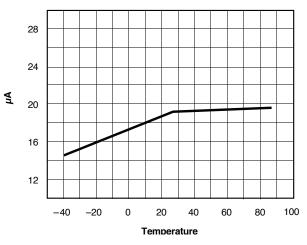
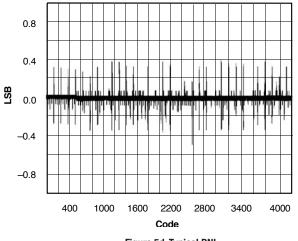


Figure 5b. Offset Current Over temperature





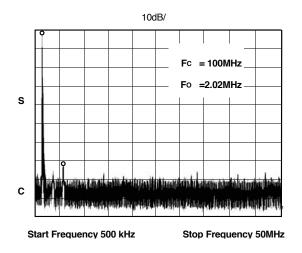


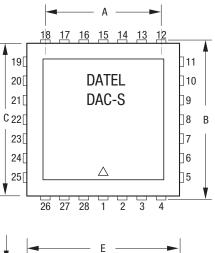
Figure 5f. Spurious Free Dynamic range = 70dB

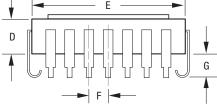


# **INPUT/OUTPUT CONNECTIONS**

PIN	FUNCTION	PIN	FUNCTION
1	D2, Digital input bit 2	28	D1 (MSB), Digital input bit 1
2	D3, Digital input bit 3	27	DGND, Digital Ground
3	D4, Digital input bit 4	26	LATCH ENABLE, Data Clock Pin (Rising Edge)
4	D5, Digital input bit 5	25	ANALOG VEE, Nomimally -5.2V
5	D6, Digital input bit 6	24	RSET, where RSET=(VREF OUT/ FS lout) x 16
6	D7, Digital input bit 7	23	DIGITAL Vcc, Nomimally +5V
7	D8, Digital input bit 8	22	REF GND, Connected closely to pin 13 & Rset ground side
8	D9, Digital input bit 9	21	DIGITAL VEE, Nomimally -5.2
9	D10, Digital input bit 10	20	REF OUT, –1.26V connected to CTRL AMP IN (Pin 19), Can be connected to an External Ref
10	D11, Digital input bit 11	19	CONTROL AMP IN, Connected to REF OUT (Pin 20), Can be connected to an External Ref
11	D12, (LSB) Digital input bit 12	18	CONTROL AMP OUT, Usually connected to REF IN (Pin 17)
12	DIGITAL VEE, Nomimally –5.2V	17	REF IN, Usually connected to CTRL AMP OUT (Pin 18)
13	ANALOG GND, Connected closely to pin 22 & RSET ground side	16	IOUT, Complementary analog output current, Zero scale output when all "1"
14	lout, Analog output current, Full scale output when inputs all "1"	15	ANALOG VEE, Analog VEE, Nominally -5.2V

## **MECHANICAL DIMENSIONS (inches (mm))**





SYMBOL	INCHES
А	0.300
В	0.466
С	0.450
D	0.090
E	0.420
F	0.050
G	0.055

### **ORDERING INFORMATION**

MODEL	OPERATING TEMPERATURE RANGE	PACKAGE	RoHS
DAC-S/MC	0 to 70°C	28-PIN CLCC	No
DAC-S/MC-C	0 to 70°C	28-PIN CLCC	Yes
DAC-S/ME	-40 to 100°C	28-PIN CLCC	No
DAC-S/ME-C	-40 to 100°C	28-PIN CLCC	Yes
DAC-S	–55 to 125°C	28-PIN CLCC	No
DAC-S-C	–55 to 125°C	28-PIN CLCC	Yes

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