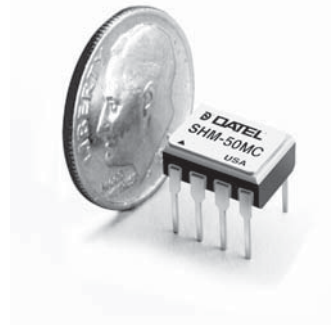


New SMT Package

FEATURES

- Small 8-pin DIP or SMT package
- 30ns typical acquisition time to $\pm 0.01\%$, 40ns typical acquisition time to 0.005%
- 15ns typical sample-to-hold settling time to $\pm 0.01\%$
- 100MHz small signal bandwidth
- -78dB feedthrough attenuation
- ± 2 picoseconds aperture uncertainty
- 85mW typical, 135mW maximum power dissipation



GENERAL DESCRIPTION

DATEL's SHM-50 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. The SHM-50 features excellent dynamic specifications including a maximum acquisition time of only 40 nanoseconds for a 2V step to $\pm 0.01\%$.

Sample-to-hold settling time, to $\pm 0.01\%$ accuracy, is 20 nanoseconds maximum with an aperture uncertainty of ± 2 picoseconds.

The SHM-50 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

INPUT/OUTPUT CONNECTIONS

Pin	Function
1	+5v Digital Supply
2	S/H Control
3	Analog Input
4	Analog Return
5	-5v Supply
6	Analog Output
7	+5v Analog Supply
8	Power Ground

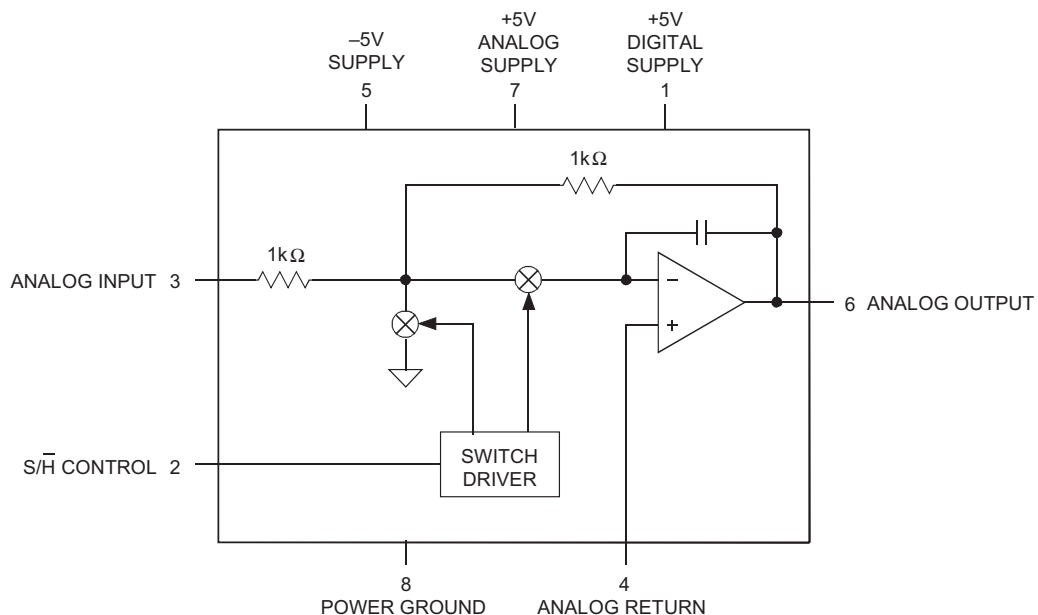


Figure 1. Functional Block Diagram

Absolute Maximum Ratings

$\pm 5V$ Supply Voltages	$\pm 6.6V$
Analog Input	$\pm 4V$
Digital Input	$-0.5V$ to $+5.5V$
Output Current	± 65 mA

Functional Specifications

Apply over the operating temperature range with $\pm 5Vdc$ unless otherwise specified.

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	-3.5	—	+3.5	Volts
Input Impedance	—	1000	—	Ω
Output Current	—	—	± 65	mA
Output Impedance	—	0.1	—	Ω
Capacitive Load	100	250	—	pF
DIGITAL INPUT				
Input Logic Levels				
Logic 1	+2.0	—	+5.0	Volts
Logic 0	0	—	+0.8	Volts
Loading				
Logic 1	—	—	+5	μA
Logic 0	—	—	-5	μA
TRANSFER CHARACTERISTICS				
Gain	—	-1	—	V/V
Gain Error, +25°C	—	± 0.05	± 0.25	%
Linearity Error ①	—	± 0.0035	± 0.005	%FS
Sample Mode Offset, +25°C	—	± 2	7	mV
Sample-to-Hold Offset (Pedestal), +25°C ②	—	± 30	60	mV
Gain Drift	—	± 1	± 15	ppm/°C
Sample Mode Offset Drift ①	—	± 3	± 15	ppm of FSR/°C
Sample-to-Hold Off. (Pedestal) Drift	—	± 5	± 20	ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time				
2V to $\pm 0.005\%$ FS ($\pm 100\mu V$)				
+25°C	—	40	50	ns
-55 to +125°C	—	70	TBD	ns
2V to $\pm 0.01\%$ FS ($\pm 200\mu V$)				
+25°C	—	30	40	ns
-55 to +125°C	—	40	50	ns
2V to $\pm 0.1\%$ FS ($\pm 2mV$)	—	25	30	ns
Sample-to-Hold Settling Time				
2V to $\pm 0.005\%$ FS ($\pm 100\mu V$)	—	15	25	ns
2V to $\pm 0.01\%$ FS ($\pm 200\mu V$)	—	10	20	ns
Sample-to-Hold Transient	—	100	—	mVp-p
Aperture Delay Time	—	2	4	ns
Aperture Uncertainty (Jitter)	—	± 2	± 4	ps
Output Slew Rate	600	± 650	—	V/ μs
Small Signal BW (-3dB)	90	100	—	MHz
Output Droop				
+25°C	—	± 0.2	± 1.0	$\mu V/nS$
0 to +70°C	—	± 0.3	± 1.0	$\mu V/nS$
-55 to +125°C	—	± 5.0	± 12.0	$\mu V/nS$
Feedthrough Rejection	—	-78	—	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Voltage Range				
+5V Supply	+4.75	+5.0	+5.25	Volts
-5V Supply	-4.75	-5.0	-5.25	Volts
Power Supply Rejection Ratio	—	± 0.5	± 1	mV/V
Quiescent Current Drain				
+5V Analog Supply	—	+7	+12	mA
-5V Supply	—	-10	-15	mA
Power Consumption	—	85	135	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-50MC				0 to +70°C
SHM-50MM				-55 to +125°C
Storage Temperature Range				
-65 to +150°C				
Thermal Impedance				
θ_{jc}				15°C/W
θ_{ca}				35°C/W
Package Type	8-pin ceramic DIP or SMT			

Footnotes:

- ① Full Scale (FS) = 2V. Full Scale Range (FSR) = 4V.
- ② Sample-to-hold offset error (pedestal) is constant regardless of input/output level.

Ordering Information

MODEL	OPERATING TEMP. RANGE	PACKAGE
SHM-50MC	0 to +70°C	DIP
SHM-50MM	-55 to +125°C	DIP
SHM-50GC	0 to +70°C	SMT
SHM-50GM	-55 to +125°C	SMT

For availability of high-reliability versions of the SHM-50, contact DATEL.

TECHNICAL NOTES

1. All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Take care to ensure that no ground potentials can exist between ground pins. A single +5V supply can be used for both +5V Digital Supply (pin 1) and +5V Analog Supply (pin 7).
2. External 0.1 μF to 4.7 μF tantalum bypass capacitors are required in critical applications.
3. A logic 1 on S/H puts the unit in the sample mode. A logic 0 puts the unit in hold mode.
4. Gain and offset adjusting can be accomplished using the external circuitry shown in Figure 2. Adjust offset with a 0V input. Adjust gain with a $\pm FS$ input. Adjust so that the output in the hold mode matches the input.

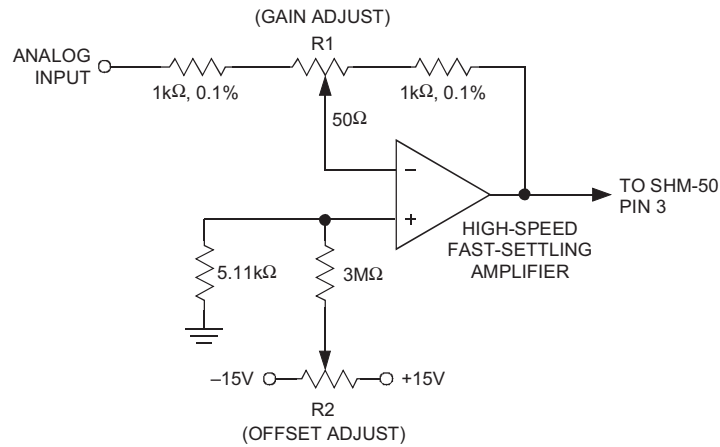
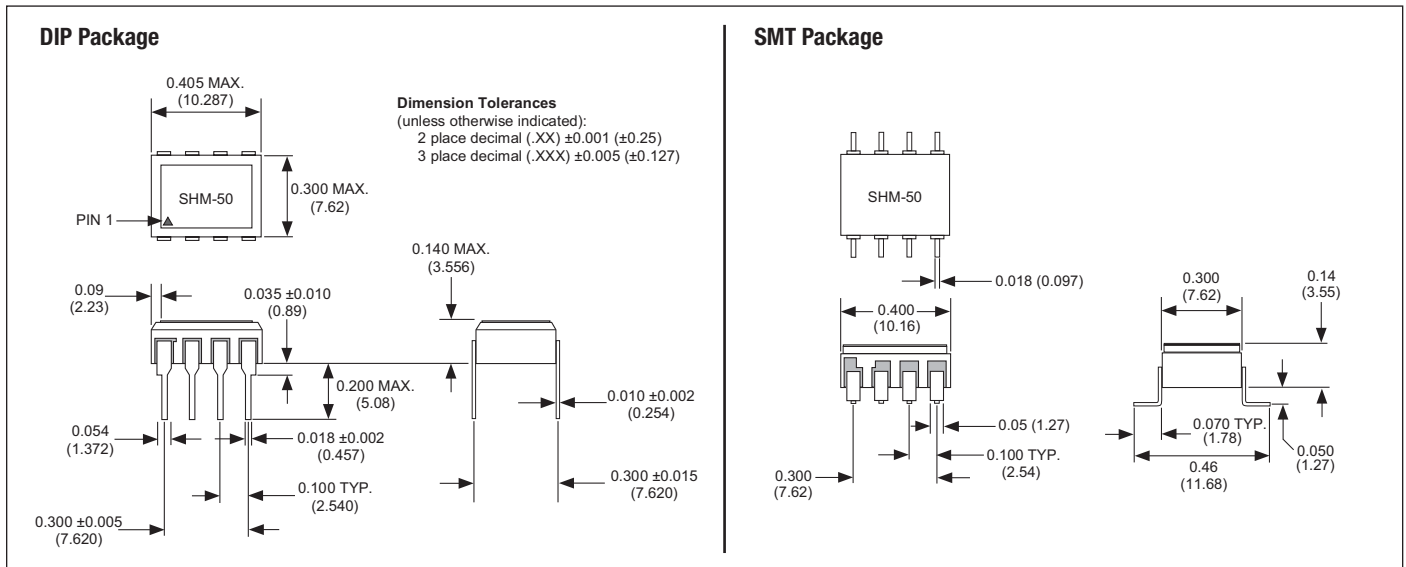


Figure 2. Offset and Gain Adjustments

MECHANICAL DIMENSIONS Inches (mm)



ISO 9001
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