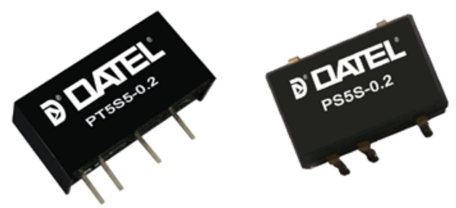


PRODUCT OVERVIEW

The PT/PS series offer 1 watts of isolated output power in an 8 pin SIP standard package or SMD package. These converters have input ranges of 5, 12, and 24 volts with a 10% tolerance. They provide precise unregulated output voltage ranging from 3.3 to 15 volts. The output voltage can be single or dual depending on the model. Other output voltages are also available and please contact DATEL if your application requires such modification.

This series features high efficiency up to 83%; 1500Volts of DC of isolation and can operate over the ambient temperature range of –40°C to +85°C. These modules offer low noise and ripple.

FEATURES

- Industry Standard SIP or SMD Package
- 1 Watts of Output power
- 1500 Volts DC of isolation
- 10% input voltage ranges (5, 12, 24 Volts)
- Unregulated Outputs
- Up to 83 % Efficiency
- -40°C to +85°C temperature range
- No Tantalum Capacitor is needed
- Low Noise and Ripple
- Low cost
- Designed to meet CE and UL/CSA60950

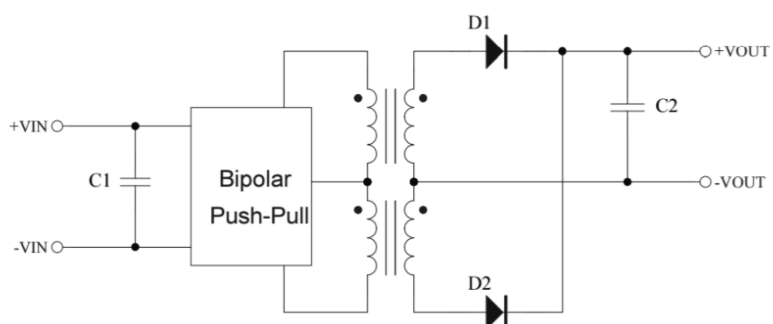
APPLICATIONS:

- Distributed Power Architectures
- Mobile telecommunication
- Industrial applications
- Battery and portable operated equipment

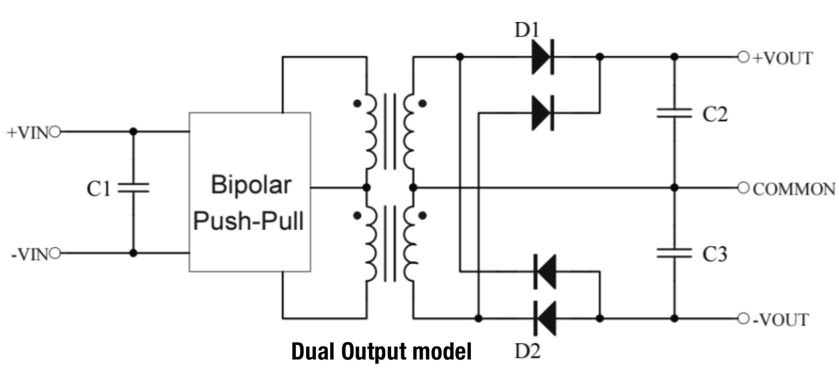
AVAILABLE OPTIONS

- SIP for all models
- SMD package for 5 and 12 volts input models
- UL/CSA60950-1, TUV per IEC/ EN60950-1, 2nd Edition

BLOCK DIAGRAM



Single Output model



Dual Output model

MODEL SELECTIONS

MODEL NUMBER	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT MAX	EFFICIENCY %	INPUT CURRENT MINIMUM	INPUT CURRENT MAXIMUM
PT5S5-0.2 or PS5S5-0.2	4.5 - 5.5V	5.0 VDC	200 mA	79	40 mA	253 mA
PT5S12-0.08 or PS5S12-0.08	4.5 - 5.5V	12 VDC	84 mA	79	40 mA	255 mA
PT5S15-0.06 or PS5S15-0.06	4.5 - 5.5V	15 VDC	67 mA	79	40 mA	254 mA
PT5D9-0.05 or PS5D9-0.05	4.5 - 5.5V	±9.0 VDC	55 mA	78	40 mA	258 mA
PT5D12-0.04 or PS5D12-0.04	4.5 - 5.5V	±12 VDC	±42 mA	78	40 mA	258 mA
PT5D15-0.03 or PS5D15-0.03	4.5 - 5.5V	±15 VDC	±33 mA	78	40 mA	258 mA
PT5D5-0.1 or PS5D5-0.1	4.5 - 5.5V	±5.0 VDC	±100 mA	74	40 mA	270 mA
PT12S5-0.2 or PS12S5-0.2	10.8 – 13.2	5.0 VDC	200 mA	80	15 mA	104 mA
PT12S12-0.08 or PS12S12-0.08	10.8 – 13.2	12 VDC	84 mA	81	15 mA	104 mA
PT12S15-0.06 or PS12S15-0.06	10.8 – 13.2	15 VDC	67 mA	81	15 mA	103 mA
PT12D12-0.04 or PS12D12-0.04	10.8 – 13.2	±12 VDC	±42 mA	80	15 mA	105 mA
PT12D15-0.03 or PS12D15-0.03	10.8 – 13.2	±15 VDC	±33 mA	81	15 mA	102 mA
PT12D5-0.1 or PS12D5-0.1	10.8 – 13.2	±5 VDC	±100 mA	77	15 mA	108 mA
PT24S5-0.2	21.6 – 26.4V	5.0 VDC	200 mA	80	7 mA	52 mA
PT24S12-0.08	21.6 – 26.4V	12 VDC	84 mA	83	7 mA	51 mA
PT24S15-0.06	21.6 – 26.4V	15 VDC	67 mA	81	7 mA	52 mA
PT24D12-0.04	21.6 – 26.4V	±12 VDC	±42 mA	81	7 mA	52 mA
PT24D15-0.03	21.6 – 26.4V	±15 VDC	±33 mA	82	7 mA	50 mA
PT24D5-0.1	21.6 – 26.4V	±5 VDC	±100 mA	79	7 mA	53 mA

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITIONS	MODEL	Min.	Typical	Max.	Units
Input Voltage						
Continuous	DC	$5V_{in}$ $12V_{in}$ $24V_{in}$	-0.7 -0.7 -0.7		5.5 13.2 26.4	Volts
Transient	100ms, DC	5Vin 12Vin $24V_{in}$			9 18 30	Volts
Operating Ambient Temperature	Derating, Above 70°C	All	-40		+85	°C
Case Temperature		All	-40		+100	°C
Storage Temperature		All	-55		+125	°C
Input / Output Isolation Voltage	1 minute	All	1500			Volts

INPUT CHARACTERISTICS

Note: All specifications are typical at nominal input, full load at 25°C unless otherwise noted

PARAMETER	CONDITIONS	MODEL	Min.	Typical	Max.	Units
Operating Input Voltage		5Vin 12Vin $24V_{in}$	4.5 10.8 21.6	5 12 24	5.5 13.2 26.4	Volts
Maximum Input Current	Full Load, Vin =4.5V	5Vin			250	mA
	Full Load, Vin = 10.8V	12Vin			110	
	Full Load, Vin =21.6V	24Vin			50	
No-Load Input Current	Vin =Nominal input	5Vin		40		mA
		12Vin		15		mA
		24Vin		7		mA
Inrush Current (I^2t)	As per ETS300 132-2	All			0.01	A^2s

OUTPUT CHARACTERISTIC

PARAMETER	CONDITIONS	MODEL	Min.	Typical	Max.	Units
		Vo=5.0 Vo=12 Vo=15 Vo=±5.0 Vo=±12 Vo=±15	4.85 11.64 14.55 ±4.85 ±11.64 ±14.55	5 12 15 ±5 ±12 ±15	5.15 12.36 15.45 ±5.15 ±12.36 ±15.45	
Output Voltage Regulation						
Line Regulation	For Vin Change of 1%	Single Dual			±1.2 ±1.2	% %
Load Regulation	Io=20% to 100%	Single Dual			±10.0	% %
Cross Regulation	Load cross variation 10%/100%	Dual			±5	%
Temperature Coefficient	TC=-40°C to + 85°C				±0.05	%/°C
Output Voltage balance	Vin =Nominal Vin , Io = Io_max, Tc=25℃	Dual			±1	%
Output Voltage Ripple and Noise						
Peak-to-Peak	Full Load, 20 MHz, Output with 0.33uF Ceramic Capacitor	PT Models			75	mV
		PS Models			120	
Operating Output Current Range		Vo=5V Vo=12V Vo=15V Vo=±5V Vo=±12V Vo=±15V	0 0 0 0 0 0		200 84 67 ±100 ±42 ±33	mA
Over Load	Vin=Nominal Vin, Output Voltage within Vo Set Point ±5%			120		%
Output Short Circuit	Momentary	All			1	Sec
Maximum Output Capacitance	Full load, Resistance	Vo=5V Vo=12V Vo=15V Vo=±5V Vo=±12V Vo=±15V			200 200 200 100 100 100	µF

DYNAMIC CHARACTERISTICS

PARAMETER	CONDITIONS	MODEL	Min.	Typical	Max.	Units
Output Voltage Current Transient						
Step Change in Output Current	75% to 100% of I_{o_max} di/dt=0.1A/us	All			±6	%
Setting Time (within 1% $Vo_{nominal}$)		All			500	µs
Turn-On Delay and Rise Time						
Turn-On Delay Time, From On/Off Control	$V_{on/off}$ to $10\%V_{o\_set}$	All		1		ms
Turn-On Delay Time, From Input	V_{in_min} to $10\%V_{o\_set}$	All		1		ms
Output Voltage Rise Time	$10\%\ V_{o\_set}$ to $90\%\ V_{o\_set}$	All		2.5		ms

FEATURE CHARACTERISTICS

PARAMETER	CONDITIONS	Device	Min.	Typical	Max.	Units
	Vin=Nominal Vin	PT5S5-0.2 or PS5S5-0.2		79		
		PT5S12-0.08 or PS5S12-0.08		79		
		PT5S15-0.06 or PS5S12-0.06		79		
		PT5D9-0.05 or PS5D9-0.05		78		
		PT5D12-0.04 or PS5D12-0.04		78		
		PT5D15-0.03 or PS5D15-0.03		74		
		PT12S5-0.2 or PS12S5-0.2		80		
		PT12S12-0.08 or PS12S12-0.08		81		
		PT12S15-0.06 or PS12S12-0.06		81		
		PT12D12-0.04 or PS12D12-0.04		80		
		PT12D15-0.03 or PS12D15-0.03		81		
		PT12D5-0.1 or PS12D5-0.1		77		
		PT24S5-0.2		80		
		PT24S12-0.08		83		
		PT24S15-0.06		81		
		PT24D12-0.04		81		
		PT24D15-0.03		82		
		PT24D5-0.1		79		
ISOLATION CHARACTERISTICS						
Input to Output	1 minutes	All	1500			Volts
Isolation Resistance		All	1000			MΩ
Isolation Capacitance		All		500		pF
Switching Frequency		Vin=24 Volts Others		75 100		KHz
MTBF	I_o =100%of I_{o_max};Ta=25°C per MIL-HDBK-217F	All		1.5		M hours
Weight		PT24 series Others		2.7 1.8		grams

Operating Temperature Range

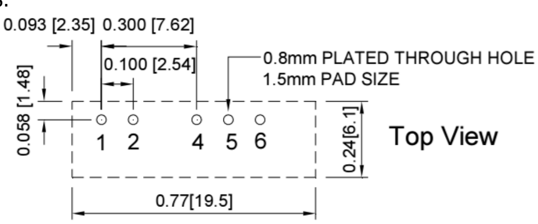
This PT/PS series of converters operate over the wide ambient temperature range from -40°C to +85°C. The case temperature should not go over +100°C during normal operating.

Output Short Circuit Protection

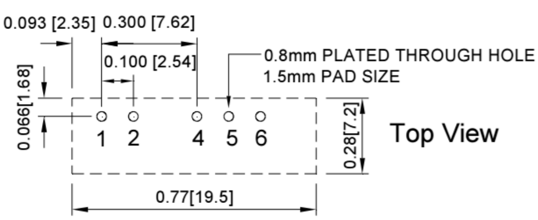
Avoid output short as much as possible because this series of converters have a momentary short-circuit protection (1 Second maximum).

Recommended PCB Layout/Footprints and Soldering Information

The user must ensure that other components and metal in the vicinity of the converter meet the spacing requirements to which the system is approved. Low resistance and low inductance PCB layout should be used where possible. Proper attention must also be given to low impedance tracks between power module, input and output grounds. The recommended footprints and soldering profiles are shown in the next two figures.



For 5Vin and 12Vin Model

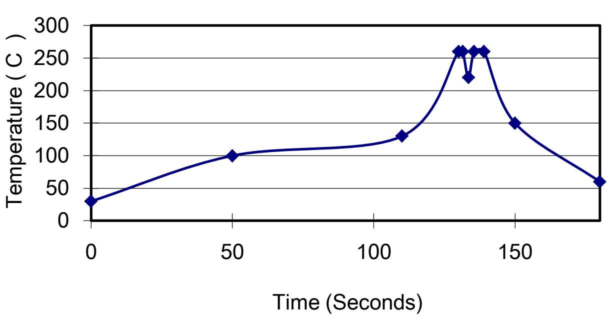


For 24Vin Model

Recommended PCB Layout Footprints

Note: Dimensions are in inches (millimeters)

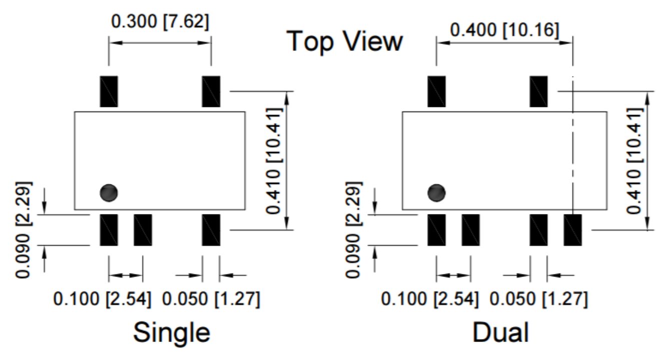
Lead Free Wave Soldering Profile



Recommended Wave Soldering Profiles for SIP models

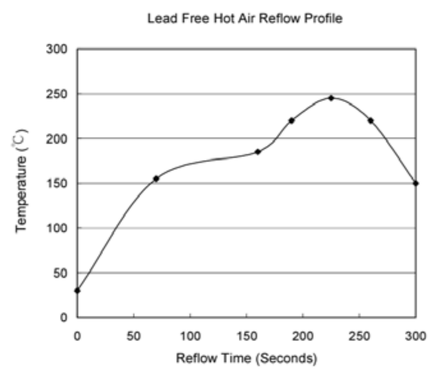
Note：

1. Soldering Materials: Sn/Cu/Ni
2. Ramp up rate during preheating: 1.4 °C/Sec (From +50°C to +100°C)
3. Soaking temperature: 0.5 °C/Sec (From +100°C to +130°C), 60 ± 20 seconds
4. Peak temperature: +260°C, above +250°C 3~6 Seconds
5. Ramp up rate during cooling: -10.0 °C/Sec (From +260°C to +150°C)



Note: Dimensions are in inches (millimeters)

Recommended PCB Layout/Footprints



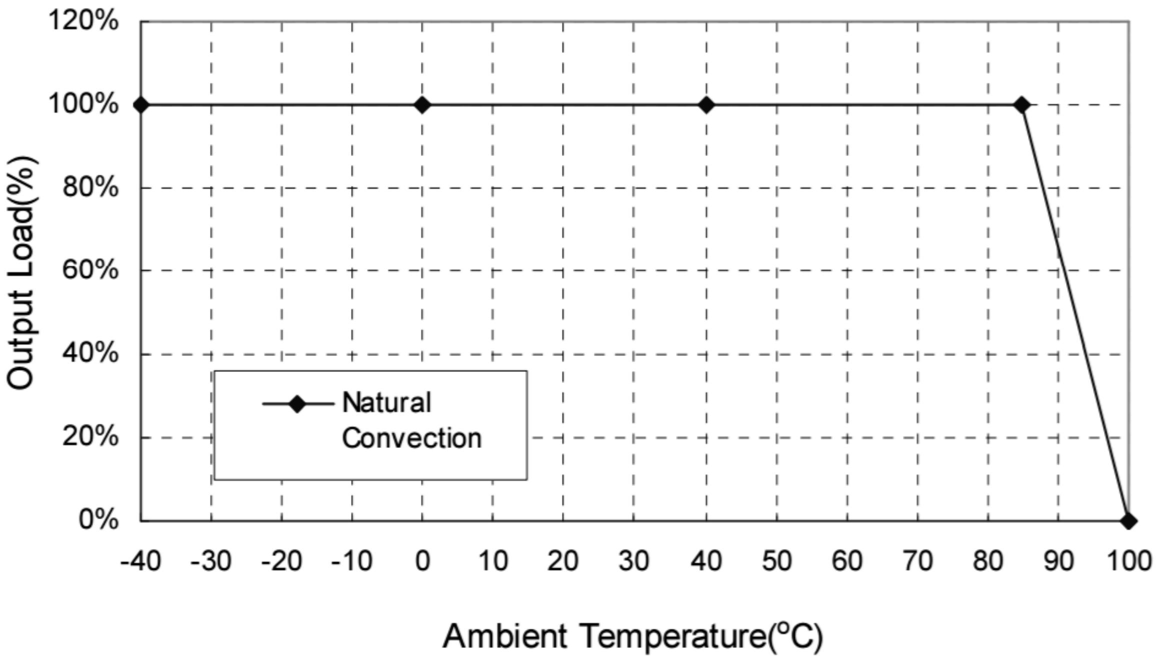
Note:

1. Soldering Paste: SHENMAO PF610-P (Sn/Ag/Cu)
2. Ramp up rate during preheat: 1.79℃/Sec (From 30℃ to 155℃)
3. Soaking temperature: 0.33℃/Sec (From 155℃ to 18℃)
4. Ramp up rate during reflow: 0.71℃/Sec (From 220℃ to 245℃)
5. Peak temperature: 245℃(10Sec max), above 220℃ 40 to 70 Seconds
6. Ramp up rate during cooling: -1.75 ℃/Sec (From 220℃ to 150℃)

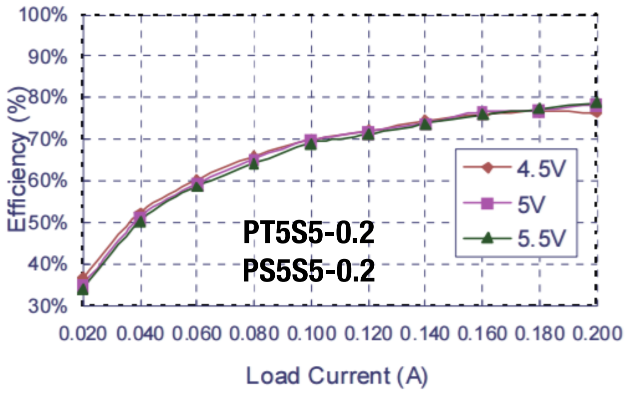
Recommended soldering profiles for SMD models

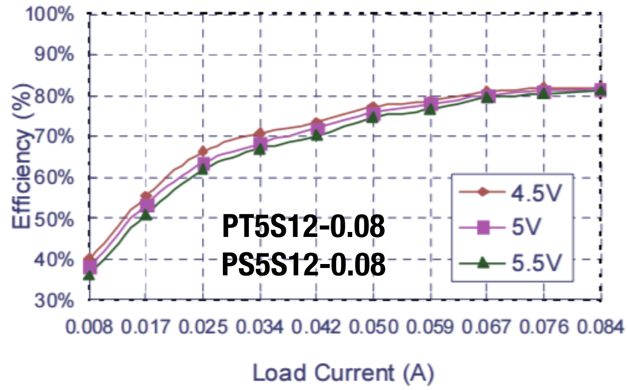
Power De-Rating Curves for PT Series

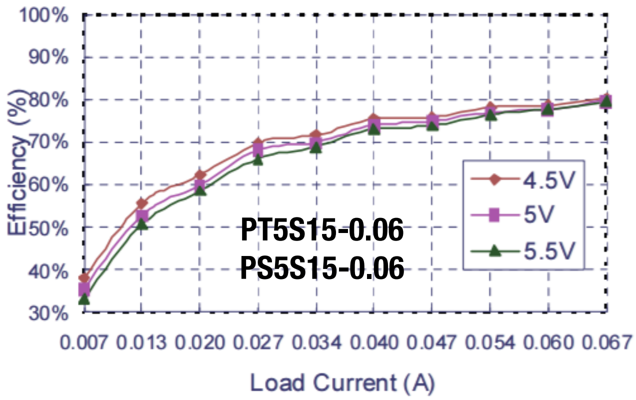
Note that the operating ambient temperature range is -40°C to + 85°C with derating above +85°C. It is recommended that the maximum case temperature under any operating condition should not exceed +100℃.

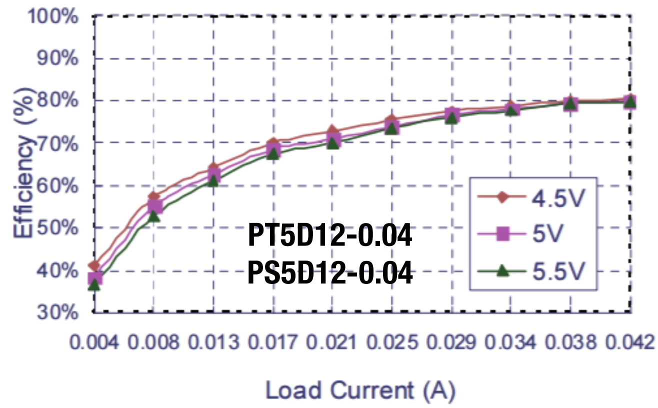


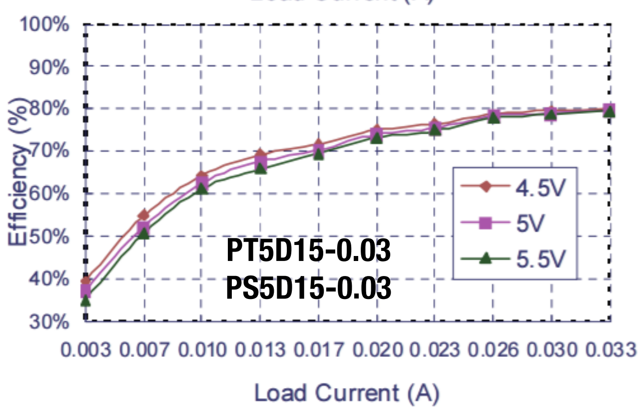
Efficiency vs. Load Curves

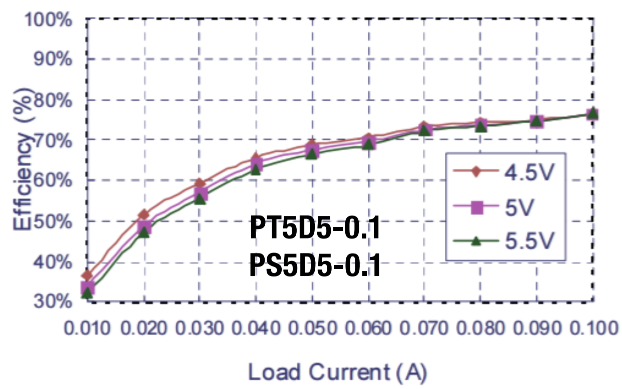




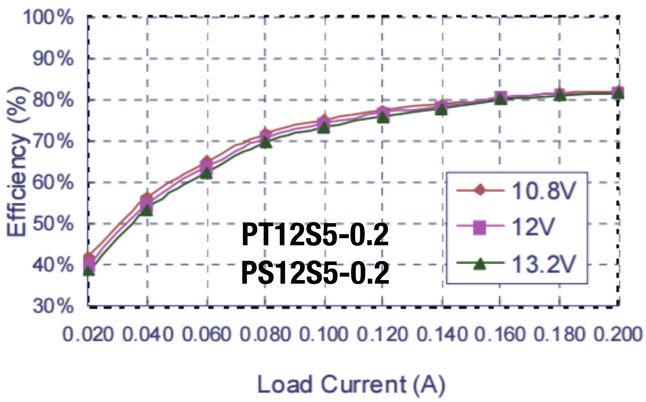


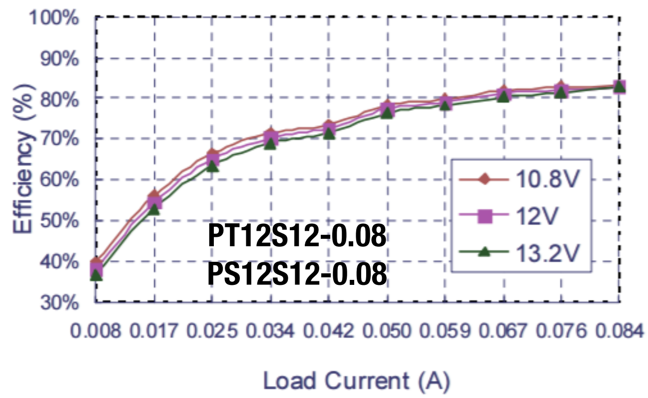


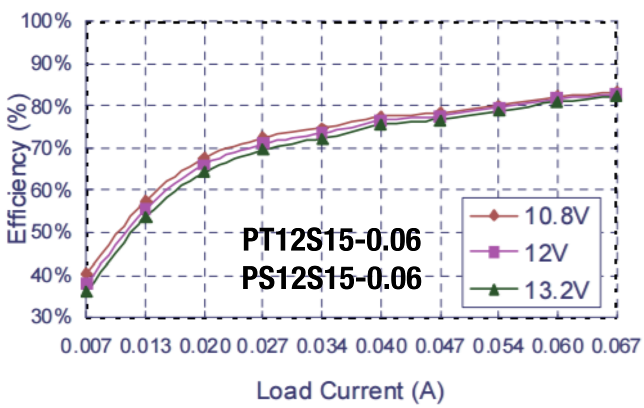


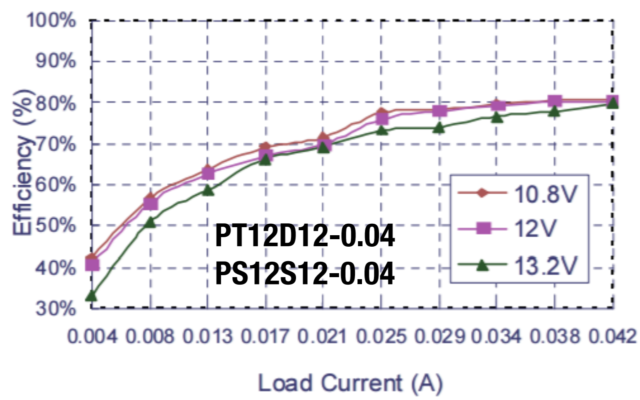


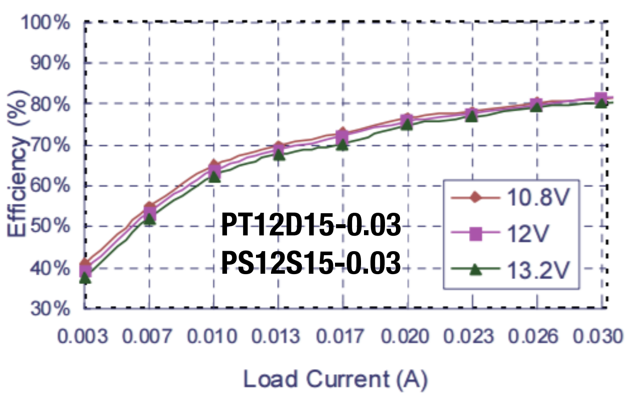
Efficiency vs. Load Curves

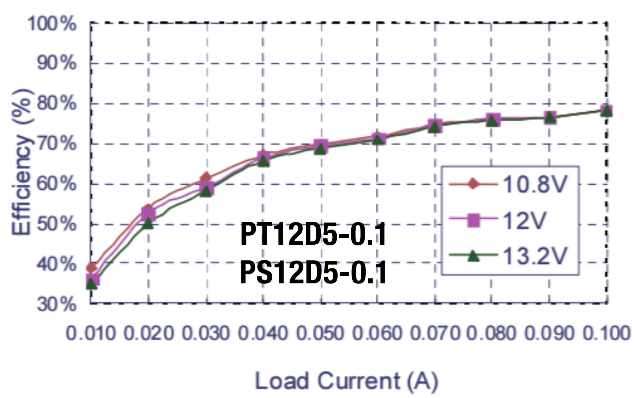




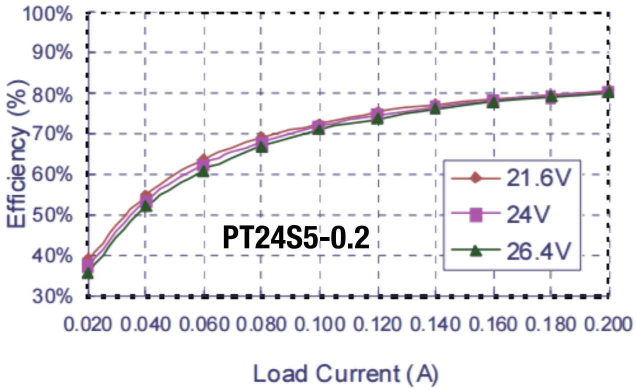


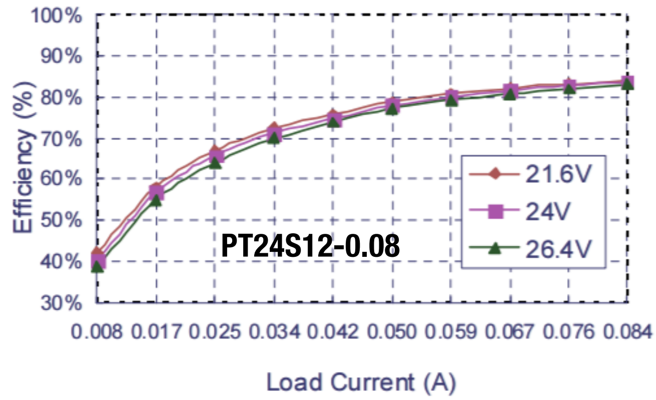


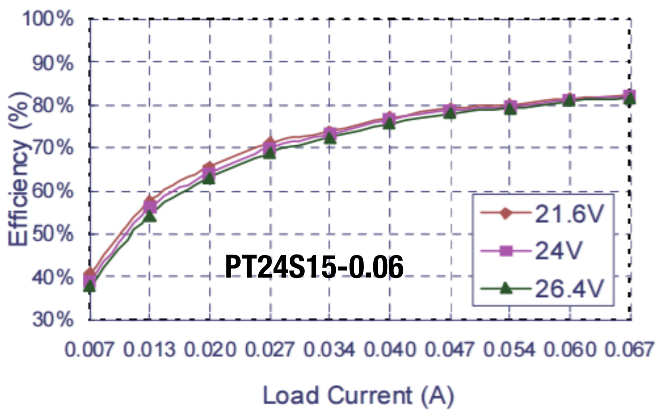


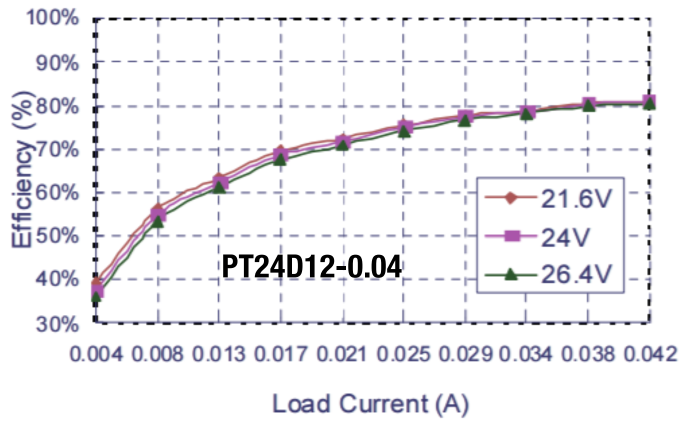


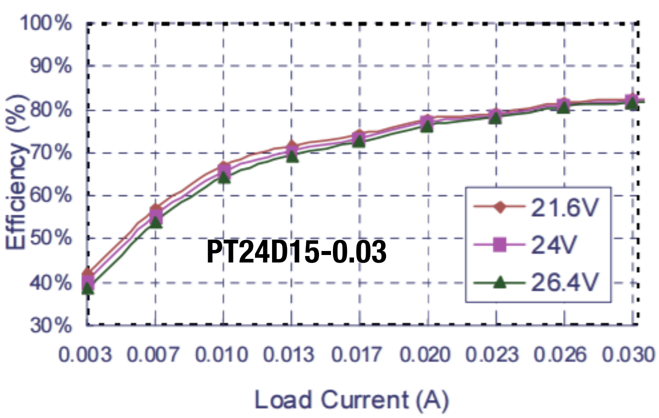
Efficiency vs. Load Curves

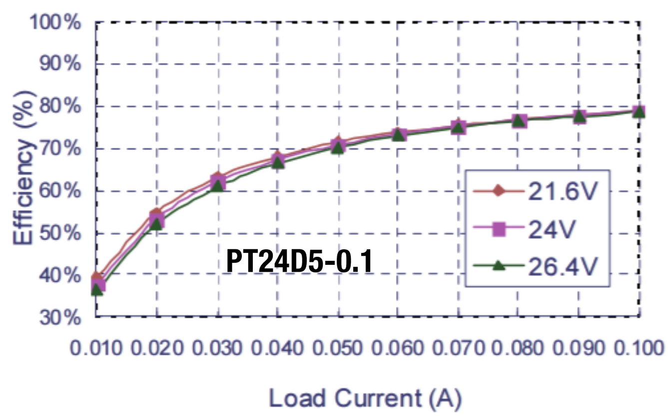






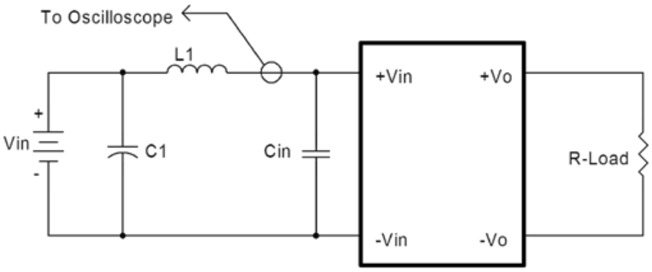






Input Capacitance at the Power Module

In order to avoid problems with loop stability, the converter must be connected to a low impedance AC source and a low inductance source. The input capacitors (Cin) should be placed close to the converter input pins to de-couple distribution inductance. The external input capacitors should have low ESR in order to quiet any ripple. Circuit as shown in the figure below represents typical measurement methods for reflected ripple current The recommended input capacitors (Cin) should be low ESR capacitors for 5Vin and 12Vin models of 2.2μF, and 4.7μF for 24Vin model. Circuit as shown in the figure below represents typical measurement methods for reflected ripple current. C1 and L1 simulate a typical DC source impedance. The input reflected-ripple current is measured by a current probe oscilloscope with a simulated source Inductance (L1).



L1: 12uH
C1: 2.2uF or 4.7uF Tantalum capacitor
Cin: None

Input Reflected-Ripple Test Setup

Test Set-Up

The basic test set-up to measure efficiency, load regulation, line regulation and other parameters is shown in the next figure. When testing the converter under any transient conditions, the user should ensure that the transient response of the source is sufficient to power the equipment under test. Below is the calculation of:

1- Efficiency
2- Load regulation
3- Line regulation

The value of efficiency is defined as:

$$\eta = \frac{V_O \times I_O}{V_{IN} \times I_{IN}} \times 100\%$$

Where

V_O is output voltage,
I_O is output current,
V_{IN} is input voltage,
I_{IN} is input current.

The value of load regulation is defined as:

$$Load.reg = \frac{V_{FL} - V_{NL}}{V_{NL}} \times 100\%$$

Where

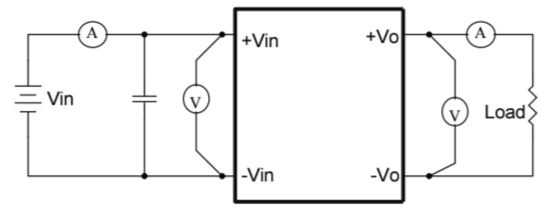
V_{FL} is the output voltage at full load
V_{NL} is the output voltage at 20% load

Line regulation is per 1.0% change in input voltage

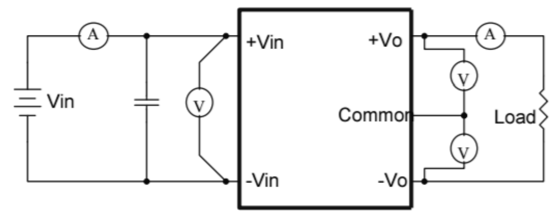
The value of line regulation is defined as:

$$Line.reg = \frac{\frac{V_{HL} - V_{LL}}{V_{NOM}} \times 100\%}{20}$$

Where: V_{HL} is the output voltage of maximum input voltage at full load.
V_{LL} is the output voltage of minimum input voltage at full load.
V_{NOM} is the output voltage of nominal input voltage at full load.



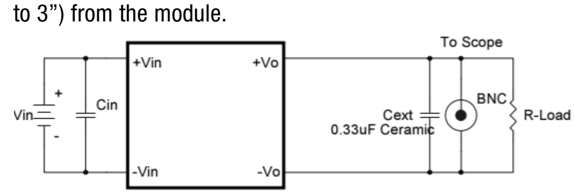
PT/PS Series Single output Test Setup



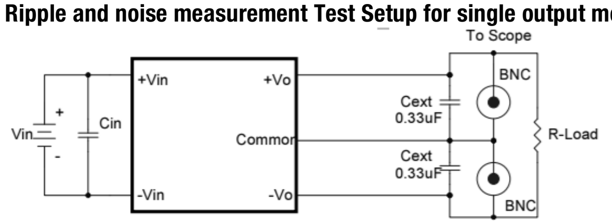
PT/PS Series Dual output Test Setup

Output Ripple and Noise Measurement

The test set-up for noise and ripple measurements is shown inthe two figures below. A coaxial cable was used to prevent impedance mismatch reflections disturbing the noise readings at higher frequencies. Measurements are taken with output appropriately loaded and all ripple/noise specifications are from D.C. to 20MHz Band Width. The output ripple/noise is measured with 0.33uF ceramic capacitor across output. The ripple and noise is measured by BNC at 50mm to 75mm (2” to 3”) from the module.



Ripple and noise measurement Test Setup for single output models



Ripple and Noise Measurement Set-Up for dual output models

Note for 5Vin, 12Vin models Cin with 2.2μF ceramic capacitor. * For 24Vin models Cin with 4.7μF ceramic capacitor.

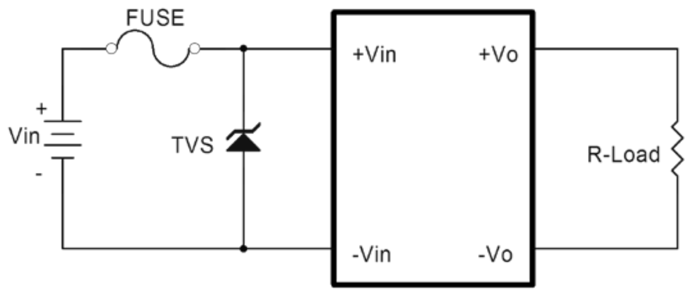
Output Capacitance

The PT/PS series of converters provide unconditional stability with or without external capacitors. For good transient response, low ESR output capacitors should be located closer to the point of load.

SAFETY and EMC

Input Fusing and Safety Considerations

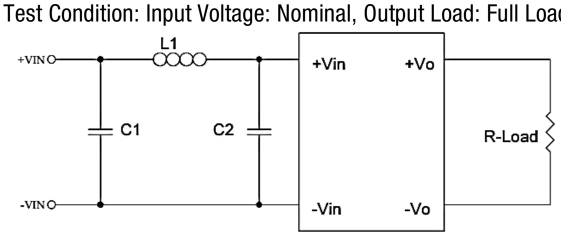
The PT series of converters do not have an internal fuse. In order to achieve maximum safety and system protection, always use an input line fuse. We recommended a time delay fuse 0.5A for all models. The circuit in the figure below is recommended and it uses a Transient Voltage Suppressor diode across the input terminal to protect the unit against surge or spike voltage and input reverse voltage.



Input Protection

EMC Considerations

EMI Test standard: EN55022 Class B Conducted Emission
Test Condition: Input Voltage: Nominal, Output Load: Full Load

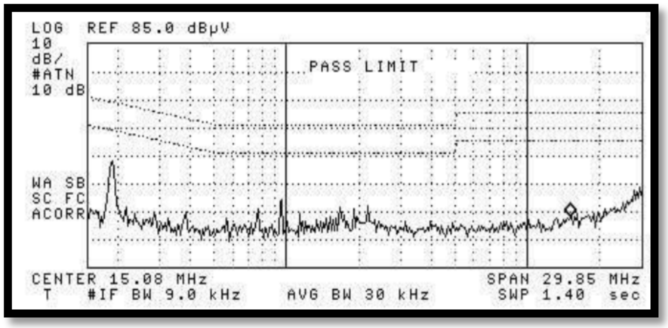


Connection circuit for conducted EMI testing

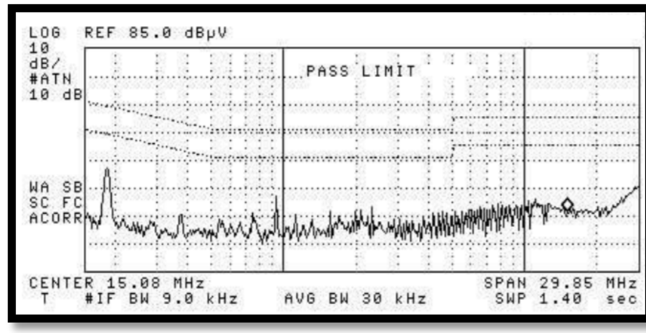
	EN55022 class B		
Model No.	**C1**	**C2**	**L1**
PT/PS5S5-0.2	4.7µF/25V	4.7µF/25V	10µH
PT/PS512-0.08	4.7µF/25V	4.7µF/25V	10µH
PT/PS5S15-0.06	4.7µF/25V	4.7µF/25V	10µH
PT/PS5D5-0.1	4.7µF/25V	4.7µF/25V	10µH
PT/PS5D9-0.05	4.7µF/25V	4.7µF/25V	10µH
PT/PS5D12-0.04	4.7µF/25V	4.7µF/25V	10µH
PT/PS5D15-0.03	4.7µF/25V	4.7µF/25V	10µH
PT/PS12S5-0.2	4.7µF/25V	4.7µF/25V	10µH
PT/PS12S12-0.08	4.7µF/25V	4.7µF/25V	10µH
PT/PS12S15-0.06	4.7µF/25V	4.7µF/25V	10µH
PT/PS12D5-0.1	4.7µF/25V	4.7µF/25V	10µH
PT/PS12D12-0.04	4.7µF/25V	4.7µF/25V	10µH
PT/PS12D15-0.03	4.7µF/25V	4.7µF/25V	10µH
PT24S5-0.2	10µF/50V	10µF/50V	7.5µH
PT2412-0.08	10µF/50V	10µF/50V	7.5µH
PT24S15-0.06	10µF/50V	10µF/50V	7.5µH
PT24D5-0.1	10µF/50V	10µF/50V	7.5µH
PT24D12-0.04	10µF/50V	10µF/50V	7.5µH
PT24D15-0.03	10µF/50V	10µF/50V	7.5µH

Note: All of capacitors are ceramic capacitors

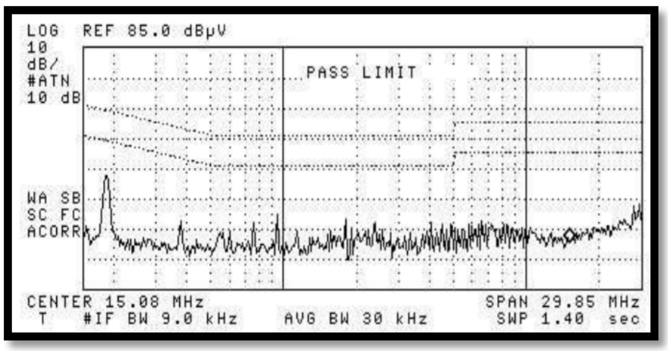
EMI and conducted noise meet EN55022 Class B



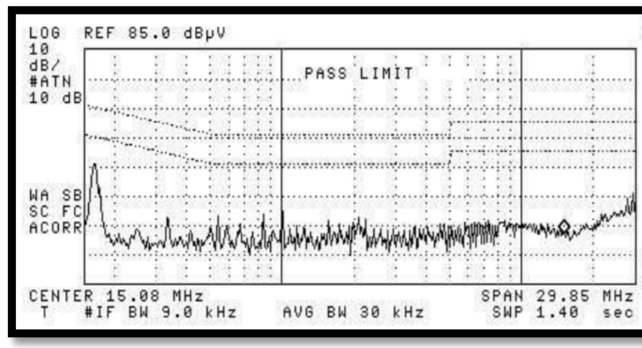
Class B Test conducted for PT/PS5S5-0.2



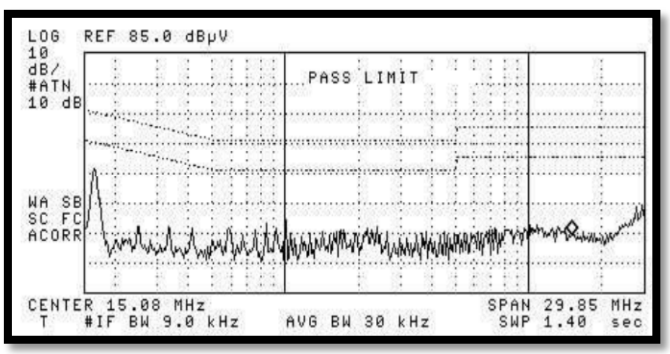
Class B Test conducted for PT/PS5S12-0.08



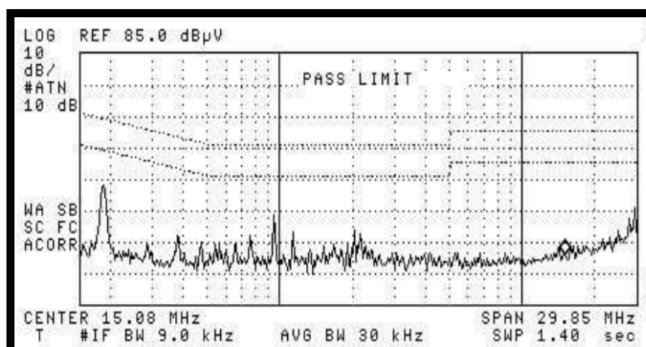
Class B Test conducted for PT/PS5S15-0.06



Class A Test conducted for PT/PS5D12-0.04

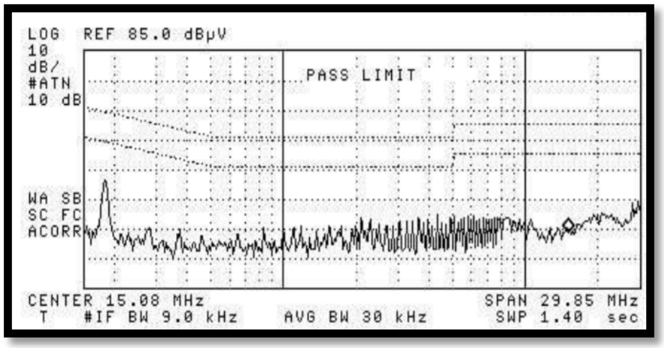


Class B Test conducted for PT/PS5D15-0.03

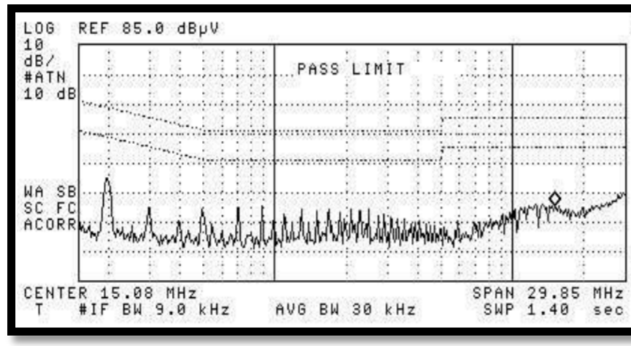


Class B Test conducted for PT/PS5D5-0.1

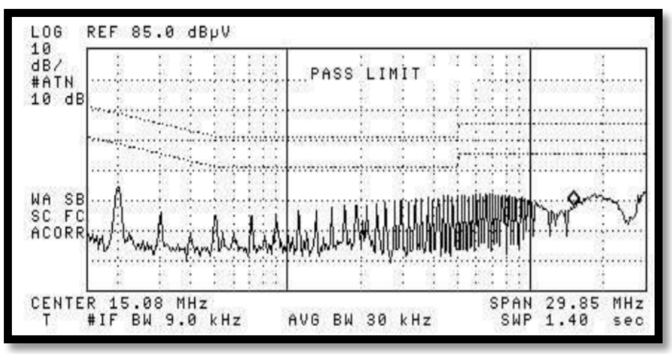
EMI and conducted noise meet EN55022 Class B



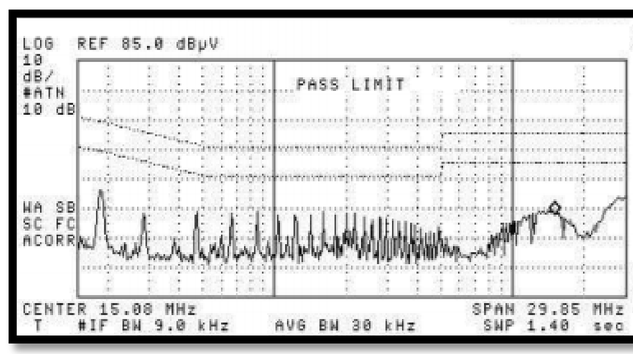
Class B Test conducted for PT/PS12S5-0.2



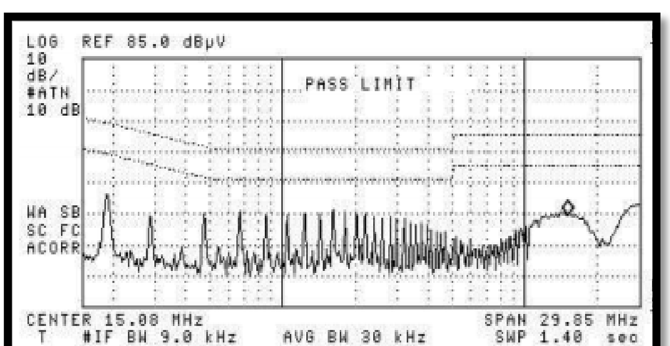
Class B Test conducted for PT/PS12S12-0.08



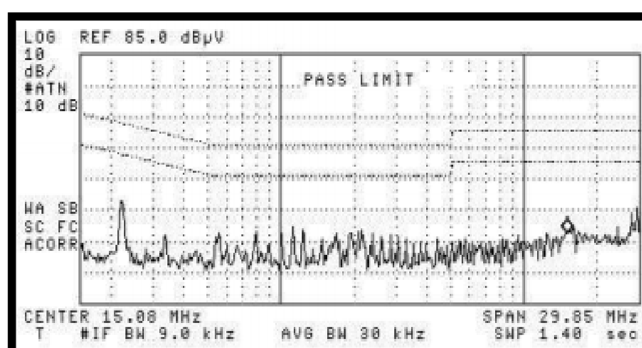
Class B Test conducted for PT/PS12S15-0.06



Class A Test conducted for PT/PS12D12-0.04

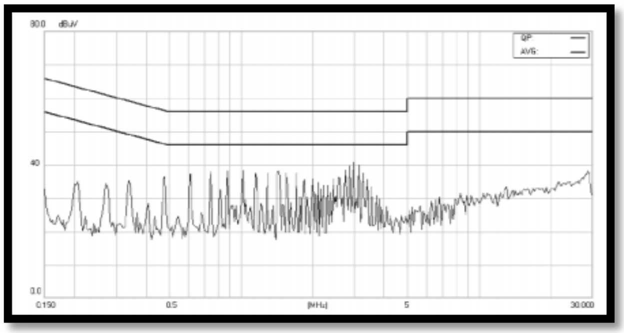


Class B Test conducted for PT/PS12D15-0.03

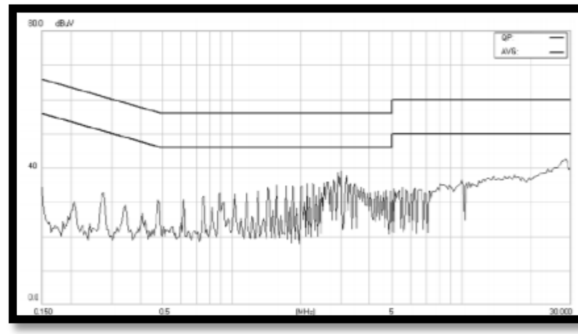


Class B Test conducted for PT/PS12D5-0.1

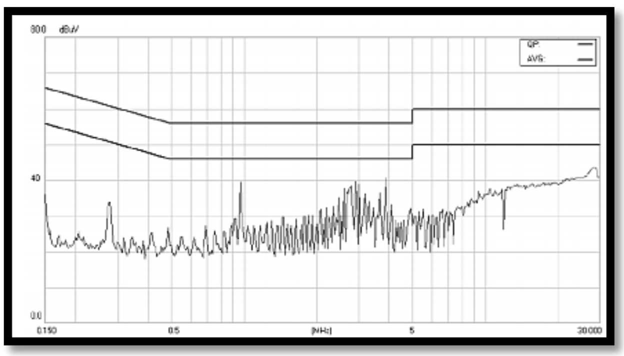
EMI and conducted noise meet EN55022 Class B



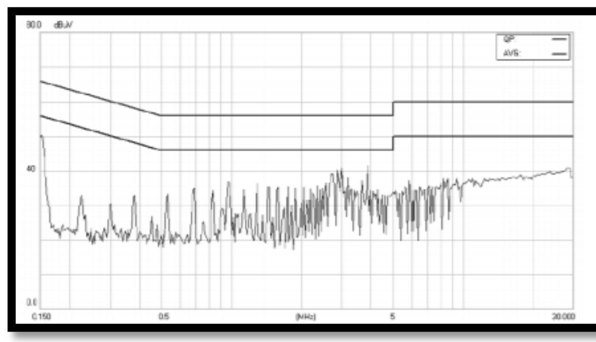
Class B Test conducted for PT24S5-0.2



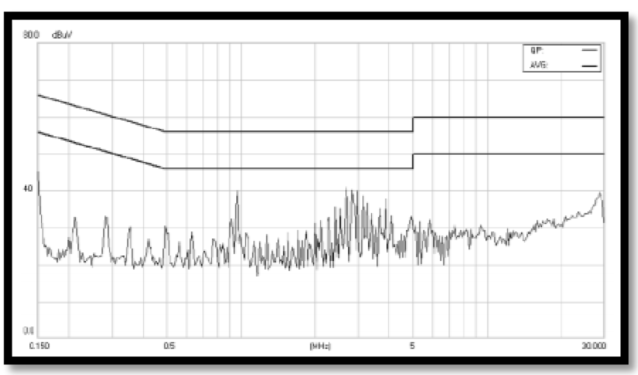
Class B Test conducted for PT24S12-0.08



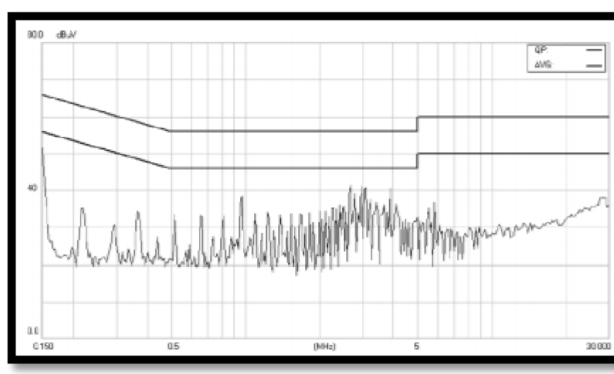
Class B Test conducted for PT24S15-0.06



Class A Test conducted for PT/PS12D12-0.04



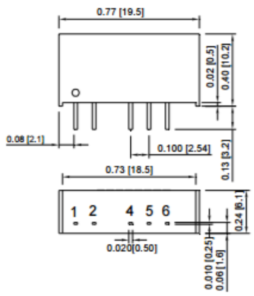
Class B Test conducted for PT24D15-0.03

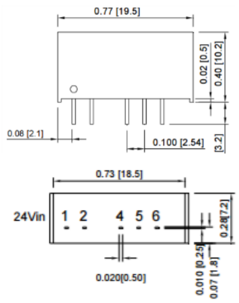


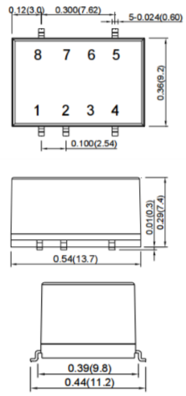
Class B Test conducted for PT24D5-0.1

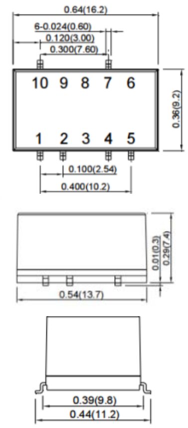
MECHANICAL SPECIFICATIONS

Note: All dimensions are in millimeters (inches). Tolerance: x.xx ±0.01 in.(0.25mm), x.xxx ±0.005 in.(0.125 mm) and for pins ±0.002 in (±0.005) are unless otherwise noted









PT5 & PT12 series | **PT24 series** | **PS5 & PS12 S series single output** | **PS5 & PS12 S series dual output**

PIN CONNECTIONS

PIN CONNECTIONS PT Series (SIP)				PIN CONNECTIONS PS Series (SMD)			
PIN	SINGLE OUTPUT	PIN	DUAL OUTPUTS	PIN	SINGLE OUTPUT	PIN	DUAL OUTPUTS
1	+ V Input	1	+ V Input	1	- V Input	1	- V Input
2	-V Input	2	-V Input	2	+V Input	2	+V Input
3	-V Output	3	-V Output	3	No Pin	3	No Pin
4	No Pin	4	No Pin	4	-V Output	4	Common
5	No Pin	5	Common	5	+V Output	5	-V Output
6	+V Output	6	+V Output	6	No Pin	6	No Pin
7	No Pin	7	No Pin	7	No Pin	7	+V Output
8	No Pin	8	No Pin	8	No Connection	8	No Pin
9	No Pin	9	No Pin	9	No Pin	9	No Pin
10	No Pin	10	No Pin	10	No Pin	8,9	No Connection

PART NUMBER ORDERING INFORMATION

Family, Form Factor	Nominal Input voltage	Number of Outputs	Voltage Output Volts		Current Output (A)
PT	**12**	**S**	**5**	—	**0.2**
PT - SIP PS - SMD	(4.5-5.5 Volts) - 5 (10.8-13.2 Volts) -12 (21.6 – 26.4 Volts) - 24	S- Single D- Dual	5 Volts – 5 ±9 Volts – 9 12 Volts – 12 15 Volts – 15 ±5 Volts - 5 ±12 Volts - 12 ±15 Volts - 15		5 Volts – 0.2 ±9 Volts – 0.05 12 Volts – 0.08 15 Volts – 0.06 ±5 Volts - 0.1 ±12 Volts - 0.04 ±15 Volts - 0.03

Note: For proper part ordering, enter option suffixes in order listed in table above