

FEATURES

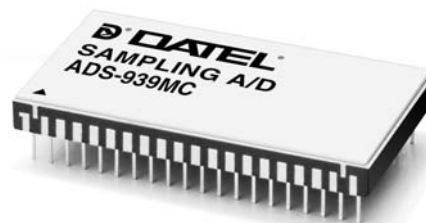
- 16-bit resolution
- 10MHz sampling rate
- Functionally complete
- No missing codes over full military temperature range
- Edge-triggered
- $\pm 5V$, $\pm 12V$ or $\pm 15V$ supplies, 1.5 Watts
- Small, 40-pin, ceramic TDIP
- 82dB SNR, $-86dB$ THD
- Ideal for both time and frequency-domain applications

GENERAL DESCRIPTION

The ADS-939 is a 16-bit, 10MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-939 has been optimized to achieve a signal-to-noise ratio (SNR) of 82dB and a total harmonic distortion (THD) of $-86dB$.

Packaged in a 40-pin TDIP, the functionally complete ADS-939 contains a fast-settling sample-and-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-939 only requires the rising edge of the start convert pulse to operate.

Requiring $\pm 5V$ supplies and either $\pm 12V$ or $\pm 15V$ supplies the ADS-939 dissipates 3.0 Watts. The device is offered with a bipolar ($\pm 2.75V$) or a unipolar (0 to $-5.5V$) analog input range. Models are available for use in either commercial (0 to $+70^{\circ}C$) or military (-55 to $+125^{\circ}C$) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range. Typical applications include medical imaging, radar, sonar, communications and instrumentation.



INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|----------------|-----|--------------------|
| 1 | +3.2V REF. OUT | 40 | +12V/+15V |
| 2 | UNIPOLAR | 39 | -12V/-15V |
| 3 | ANALOG INPUT | 38 | +5V ANALOG SUPPLY |
| 4 | ANALOG GROUND | 37 | -5V SUPPLY |
| 5 | OFFSET ADJUST | 36 | ANALOG GROUND |
| 6 | GAIN ADJUST | 35 | COMP. BITS |
| 7 | DIGITAL GROUND | 34 | OUTPUT ENABLE |
| 8 | NC | 33 | OVERFLOW |
| 9 | NC | 32 | EOC |
| 10 | NC | 31 | +5V DIGITAL SUPPLY |
| 11 | NC | 30 | DIGITAL GROUND |
| 12 | START CONVERT | 29 | BIT 1 (MSB) |
| 13 | BIT 16 (LSB) | 28 | BIT 1 (MSB) |
| 14 | BIT 15 | 27 | BIT 2 |
| 15 | BIT 14 | 26 | BIT 3 |
| 16 | BIT 13 | 25 | BIT 4 |
| 17 | BIT 12 | 24 | BIT 5 |
| 18 | BIT 11 | 23 | BIT 6 |
| 19 | BIT 10 | 22 | BIT 7 |
| 20 | BIT 9 | 21 | BIT 8 |

POWER AND GROUNDING

| | |
|------------------------|-------|
| +5V ANALOG SUPPLY | 38 |
| +5V DIGITAL SUPPLY | 31 |
| -5V SUPPLY | 37 |
| ANALOG GROUND | 4, 36 |
| DIGITAL GROUND | 7, 30 |
| -12/-15V ANALOG SUPPLY | 39 |
| +12/+15V ANALOG SUPPLY | 40 |

POWER AND GROUNDING

| | |
|--------------------|----------|
| +5V ANALOG SUPPLY | 38 |
| +5V DIGITAL SUPPLY | 31 |
| -5V SUPPLY | 37 |
| ANALOG GROUND | 2, 4, 36 |
| DIGITAL GROUND | 7, 30 |
| NO CONNECTION | 39, 40 |

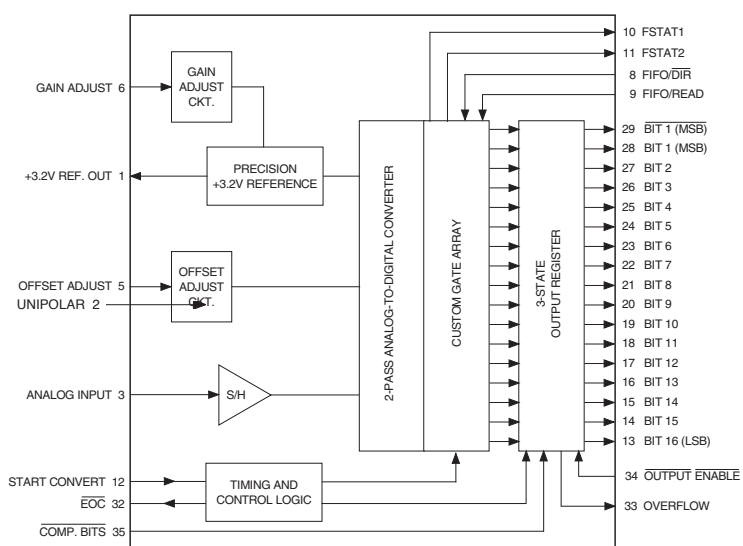


Figure 1. ADS-939 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
|--|-------------------------------|-------|
| +5V Supply (Pins 31, 38) | 0 to +6 | Volts |
| -5V Supply (Pin 37) | 0 to -6 | Volts |
| +12V/+15V Supply (pin 40) | 0 to +16V | Volts |
| -12V/-15V Supply (pin 39) | 0 to +16V | Volts |
| Digital Inputs (Pins 8, 9, 12, 34, 35) | -0.3 to +V _{DD} +0.3 | Volts |
| Analog Input (Pin 3) | ±5 | Volts |
| Lead Temperature (10 seconds) | +300 | °C |

PHYSICAL/ENVIRONMENTAL

| PARAMETERS | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|------------------------------------|------|------|---------|
| Operating Temp. Range, Case | | | | |
| ADS-939MC | 0 | — | +70 | °C |
| ADS-939MM | -55 | — | +125 | °C |
| Thermal Impedance | | | | |
| θ _{JC} | — | 4 | — | °C/Watt |
| θ _{CA} | — | 18 | — | °C/Watt |
| Storage Temperature Range | -65 | — | +150 | °C |
| Package Type | 40-pin, metal-sealed, ceramic TDIP | | | |
| Weight | 0.56 ounces (16 grams) | | | |

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±12/15V, +V_{DD} = ±5V, 10MHz sampling rate, and a minimum 3 minute warm-up ① unless otherwise specified.)

| ANALOG INPUT | +25°C | | | 0 to +70°C | | | -55 to +125°C | | | UNITS |
|---|-------|------------|------|------------|------------|------|---------------|------------|------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Input Voltage Range | | | | | | | | | | |
| Unipolar | — | 0 to -5.5V | — | — | 0 to -5.5V | — | — | 0 to -5.5V | — | Volts |
| Bipolar | — | ±2.75 | — | — | ±2.75 | — | — | ±2.75 | — | Volts |
| Input Resistance (Pin 3) | — | 400 | — | — | 400 | — | — | 400 | — | Ω |
| (Pin 2) | — | 480 | — | — | 480 | — | — | 480 | — | Ω |
| Input Capacitance | — | 10 | 15 | — | 10 | 15 | — | 10 | 15 | pF |
| DIGITAL INPUTS | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.0 | — | — | +2.0 | — | — | +2.0 | — | — | Volts |
| Logic "0" | — | — | +0.8 | — | — | +0.8 | — | — | +0.8 | Volts |
| Logic Loading "1" | — | — | +20 | — | — | +20 | — | — | +20 | μA |
| Logic Loading "0" ② | — | — | -20 | — | — | -20 | — | — | -20 | μA |
| Start Convert Positive Pulse Width ③ | 20 | 50 | — | 20 | 50 | — | 20 | 50 | — | ns |
| STATIC PERFORMANCE | | | | | | | | | | |
| Resolution | — | 16 | — | — | 16 | — | — | 16 | — | Bits |
| Integral Nonlinearity | — | ±1 | — | — | ±1.5 | — | — | ±2 | — | LSB |
| Differential Nonlinearity (f _{IN} = 10kHz) | -0.95 | ±0.5 | +1.0 | -0.95 | ±0.5 | +1.0 | -0.95 | ±0.5 | +1.5 | LSB |
| Full Scale Absolute Accuracy | — | ±0.15 | ±0.3 | — | ±0.3 | ±0.5 | — | ±0.5 | ±0.8 | %FSR |
| Bipolar Zero Error (Tech Note 2) | — | ±0.1 | ±0.2 | — | ±0.2 | ±0.4 | — | ±0.4 | ±0.6 | %FSR |
| Bipolar Offset Error (Tech Note 2) | — | ±0.1 | ±0.2 | — | ±0.2 | ±0.4 | — | ±0.4 | ±0.6 | %FSR |
| Gain Error (Tech Note 2) | — | ±0.15 | ±0.3 | — | ±0.3 | ±0.5 | — | ±0.5 | ±0.8 | % |
| No Missing Codes (f _{IN} = 10kHz) | 16 | — | — | 16 | — | — | 16 | — | — | Bits |
| DYNAMIC PERFORMANCE | | | | | | | | | | |
| Peak Harmonics (-3dB) | | | | | | | | | | |
| dc to 500kHz | — | -87 | TBD | — | -87 | TBD | — | -82 | TBD | dB |
| 500kHz to 5MHz | — | -82 | TBD | — | -82 | TBD | — | -78 | TBD | dB |
| Total Harmonic Distortion (-3dB) | | | | | | | | | | |
| dc to 500kHz | — | -86 | TBD | — | -86 | TBD | — | -81 | TBD | dB |
| 500kHz to 5MHz | — | -81 | TBD | — | -81 | TBD | — | -77 | TBD | dB |
| Signal-to-Noise Ratio | | | | | | | | | | |
| (w/o distortion, -3dB) | | | | | | | | | | |
| dc to 500kHz | TBD | 86 | — | TBD | 86 | — | TBD | 80 | — | dB |
| 500kHz to 5MHz | TBD | 85 | — | TBD | 85 | — | TBD | 80 | — | dB |
| Signal-to-Noise Ratio ④ | | | | | | | | | | |
| (& distortion, -3dB) | | | | | | | | | | |
| dc to 500kHz | TBD | 82 | — | TBD | 82 | — | TBD | 78 | — | dB |
| 500kHz to 5MHz | TBD | 81 | — | TBD | 81 | — | TBD | 75 | — | dB |
| Noise | — | 80 | — | — | 80 | — | — | 80 | — | μVrms |
| Two-Tone Intermodulation | | | | | | | | | | |
| Distortion (f _{IN} = 200kHz, 240kHz, f _S = 10MHz, -3dB) | — | -87 | -85 | — | -87 | -85 | — | -87 | -82 | dB |
| Input Bandwidth (-3dB) | | | | | | | | | | |
| Small Signal (-20dB input) | — | 25 | — | — | 25 | — | — | 25 | — | MHz |
| Large Signal (-0.5dB input) | — | 15 | — | — | 25 | — | — | 15 | — | MHz |
| Feedthrough Rejection | | | | | | | | | | |
| (f _{IN} = 1MHz) | — | 90 | — | — | 90 | — | — | 90 | — | dB |
| Slew Rate | — | ±400 | — | — | ±400 | — | — | ±400 | — | V/μs |
| Aperture Delay Time | — | 4 | — | — | 4 | — | — | 4 | — | ns |
| Aperture Uncertainty | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | ps rms |
| S/H Acquisition Time | | | | | | | | | | |
| (to ±0.001%FSR, 5.5V step) | — | 40 | — | — | 40 | — | — | 45 | — | ns |
| Overvoltage Recovery Time ⑤ | — | 100 | — | — | 100 | — | — | 100 | — | ns |
| A/D Conversion Rate | 10 | — | — | 10 | — | — | 10 | — | — | MHz |

| DYNAMIC PERFORMANCE (Cont.) | +25°C | | | 0 TO +70°C | | | -55 TO +125°C | | | UNITS |
|--|---|-------|-------|------------|---|-------|---------------|-------|-------|---------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| ANALOG OUTPUT | | | | | | | | | | |
| Internal Reference | | | | | | | | | | |
| Voltage | — | +3.2 | — | — | +3.2 | — | — | +3.2 | — | Volts |
| Drift | — | ±30 | — | — | ±30 | — | — | ±30 | — | ppm/°C |
| External Current | — | 5 | — | — | 5 | — | — | 5 | — | mA |
| DIGITAL OUTPUTS | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.4 | — | — | +2.4 | — | — | +2.4 | — | — | Volts |
| Logic "0" | — | — | +0.4 | — | — | +0.4 | — | — | +0.4 | Volts |
| Logic Loading "1" | — | — | -4 | — | — | -4 | — | — | -4 | mA |
| Logic Loading "0" | — | — | +4 | — | — | +4 | — | — | +4 | mA |
| Output Coding ⑥ | (Offset) Binary / Complementary (Offset) Binary / Two's Complement / Complementary Two's Complement | | | | | | | | | |
| POWER REQUIREMENTS | | | | | | | | | | |
| Power Supply Ranges ⑦ | | | | | | | | | | |
| +5V Supply | +4.75 | +5.0 | +5.25 | +4.75 | +5.0 | +5.25 | +4.9 | +5.0 | +5.25 | Volts |
| -5V Supply | -4.75 | -5.0 | -5.25 | -4.75 | -5.0 | -5.25 | -4.9 | -5.0 | -5.25 | Volts |
| +12V Supply ⑧ | +11.5 | +12.0 | +12.5 | +11.5 | +12.0 | +12.5 | +11.5 | +12.0 | +12.5 | Volts |
| -12V Supply ⑧ | -11.5 | -12.0 | -12.5 | -11.5 | -12.0 | -12.5 | -11.5 | -12.0 | -12.5 | Volts |
| +15V Supply ⑧ | +14.5 | +15.0 | +15.5 | +14.5 | +15.0 | +15.5 | +14.5 | +15.0 | +15.5 | Volts |
| -15V Supply ⑧ | -14.5 | -15.0 | -15.5 | -14.5 | -15.0 | -15.5 | -14.5 | -15.0 | -15.5 | Volts |
| Power Supply Currents | | | | | | | | | | |
| +5V Supply | — | +50 | — | — | TBD | — | — | TBD | — | mA |
| -5V Supply | — | -36 | — | — | TBD | — | — | TBD | — | mA |
| -12/15V Supply ⑧ | — | -25 | — | — | TBD | — | — | TBD | — | mA |
| +12/15V Supply ⑧ | — | +70 | — | — | TBD | — | — | TBD | — | mA |
| Power Dissipation | — | 1.5 | TBD | — | TBD | TBD | — | TBD | TBD | Watts |
| Power Supply Rejection | — | — | ±0.07 | — | — | ±0.07 | — | — | ±0.07 | %FSR/%V |
| Footnotes: | | | | | | | | | | |
| ① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warm-up periods. The device must be continuously converting during this time. | | | | | ⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range. | | | | | |
| ② When COMP. BITS (pin 35) is low, logic loading "0" will be -350µA. | | | | | ⑥ See table 2a, Setting Output Coding Selection. | | | | | |
| ③ A 10MHz clock with a 50nsec positive pulse width is used for all production testing. See Timing Diagram for more details. | | | | | ⑦ The minimum supply voltages of +4.9V and -4.9V for ±VDD are required for -55°C operation only. The minimum limits are +4.75V and -4.75V when operating at +125°C. | | | | | |
| ④ Effective bits is equal to: | | | | | ⑧ ±12V only or ±15V only required. | | | | | |
| $\frac{(\text{SNR} + \text{Distortion}) - 1.76}{6.02} + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}} \right]$ | | | | | | | | | | |

TECHNICAL NOTES

- Obtaining fully specified performance from the ADS-939A requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (4, 7, 30 and 36) directly to a large **analog** ground plane beneath the package. For the best performance it is recommended to use a single power source for both the +5V analog and +5V digital supplies. Bypass all power supplies and the +3.2V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.
- The ADS-939A achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warm-up. To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.
- Pin 35 (COMP. BITS) is used to select the digital output coding format of the ADS-939A. See Tables 2a and 2b. When this pin has a TTL logic "0" applied, it complements all of the ADS-939A's digital outputs. When pin 35 has a logic "1" applied, the output coding is comple-

mentary (offset) binary. Applying a logic "0" to pin 35 changes the coding to (offset) binary. Using the MSB output (pin 29) instead of the MSB output (pin 28) changes the respective output codings to complementary two's complement and two's complement.

Pin 35 is TTL compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 35 allowing it to be either connected to +5V or left open when a logic "1" is required.

- To enable the three-state outputs, connect OUTPUT ENABLE (pin 34) to a logic "0" (low). To disable, connect pin 34 to a logic "1" (high).
- Applying a start convert pulse while a conversion is in progress (EOC = logic "1") will initiate a new and probably inaccurate conversion cycle. Data from both the interrupted and subsequent conversions will be invalid.
- Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the rising edge of EOC to the falling edge of EOC).
- The OVERFLOW bit (pin 33) switches from 0 to 1 when the input voltage exceeds that which produces an output of all 1's or when the input equals or exceeds the voltage that produces all 0's. When COMP BITS is activated, the above conditions are reversed.

CALIBRATION PROCEDURE

Connect the converter per Figure 2. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuits in Figure 2 are guaranteed to compensate for the ADS-939's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting

LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-939, offset adjusting is normally accomplished when the analog input is 0 minus ½ LSB ($-42\mu\text{V}$). See Table 2b for the proper bipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1½ LSB's ($+2.749874\text{V}$ or -5.499874V).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

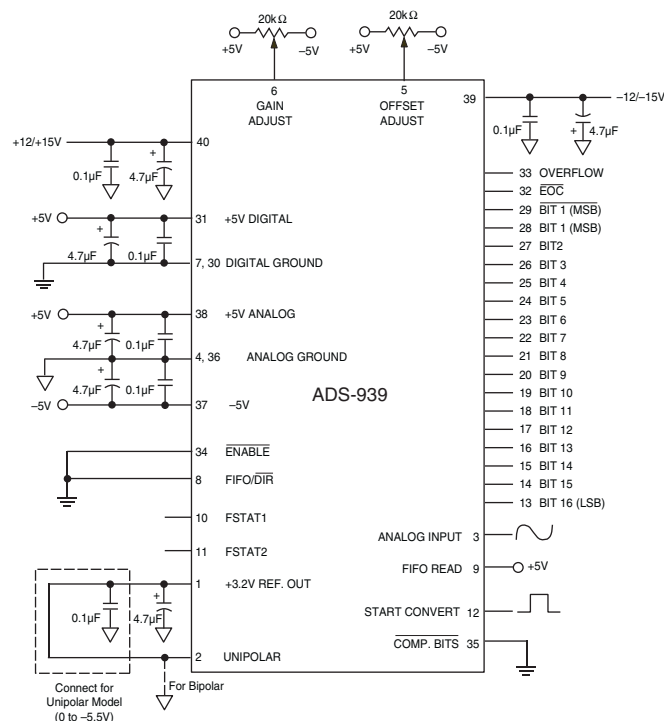


Figure 2. Connection Diagram

Table 2a. Setting Output Coding Selection (Pin 35)

| OUTPUT FORMAT | PIN 35 LOGIC LEVEL |
|--|--------------------|
| Complementary (Offset) Binary | 1 |
| (Offset) Binary | 0 |
| Complementary Two's Complement (Using MSB, pin 29) | 1 |
| Two's Complement (Using MSB, pin 29) | 0 |

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 12) so that the converter is continuously converting.
2. For zero/offset adjust, apply $-42\mu\text{V}$ to the ANALOG INPUT (pin 3).
3. For bipolar operation - Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 35 tied high (complementary offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 35 tied low (offset binary).

For unipolar operation - Adjust the offset potentiometer until all outputs are 1's and the LSB flickers between 0 and 1 with pin 35 tied high (complementary binary) or until all outputs are 0's and the LSB flickers between 0 and 1 with pin 35 tied low (binary).

4. For bipolar, Two's complement coding requires using BIT 1 (MSB) (pin 29). With pin 35 tied low, adjust the trimpot until the output code flickers between all 0's and all 1's.

Gain Adjust Procedure

1. For gain adjust, for bipolar apply $+2.749874\text{V}$ and for unipolar mode 5.499874V to the ANALOG INPUT (pin 3).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 35 tied high (complementary (offset) binary) or until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 35 tied low ((offset) binary).
3. For bipolar, Two's complement coding requires using BIT 1 (MSB) (pin 29). With pin 35 tied low, adjust the gain trimpot until the output code flickers equally between 0111 1111 1111 1111 and 0111 1111 1111 1110.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2b.

Table 2b. Output Coding

| INPUT RANGE 0 to -5.5V | UNIPOLAR SCALE | COMP. BINARY | | BINARY | | COMP. TWO'S COMP. | | TWO'S COMP. | | INPUT RANGE ±2.75V | BIPOLAR SCALE |
|---------------------------|----------------|----------------|----------------|-----------------|----------------|-------------------|----------------|-------------------|----------------|-----------------------|----------------|
| | | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | | |
| 0 -1 LSB | -0.000084 | 1111 | 1111 1111 1111 | 0000 | 0000 0000 0000 | 0111 | 1111 1111 1111 | 1000 | 0000 0000 0000 | +2.749916 | +FS -1 LSB |
| 0 -1 1/2 LSB | -0.000126 | LSB "1" to "0" | | LSB "0" to "1" | | LSB "1" to "0" | | LSB "0" to "1" | | +2.749874 | +FS -1 1/2 LSB |
| 0 - 1/8 FS | -0.687500 | 1110 | 0000 0000 0000 | 0001 | 1111 1111 1111 | 0110 | 0000 0000 0000 | 1001 | 1111 1111 1111 | +2.062500 | +3/4 FS |
| 0 - 1/4 FS | -1.375000 | 1100 | 0000 0000 0000 | 0011 | 1111 1111 1111 | 0100 | 0000 0000 0000 | 1011 | 1111 1111 1111 | +1.375000 | +1/2 FS |
| -1/2 FS -1/2 LSB | -2.749958 | 1000 | 0000 0000 0000 | 0111 | 1111 1111 1111 | 0000 | 0000 0000 0000 | 1111 | 1111 1111 1111 | 0.000000 | 0 |
| -1/2 LSB | -2.750000 | 0111 | 1111 1111 1111 | 1000 | 000 000 0000 | 1111 | 1111 1111 1111 | 0000 | 0000 0000 0000 | -0.000084 | -1 LSB |
| -3/4 FS | -4.125000 | 0100 | 0000 0000 0000 | 1011 | 1111 1111 1111 | 1100 | 0000 0000 0000 | 0011 | 1111 1111 1111 | -1.375000 | -1/2 FS |
| -7/8 FS | -4.812500 | 0010 | 0000 0000 0000 | 1101 | 1111 1111 1111 | 1010 | 0000 0000 0000 | 0101 | 1111 1111 1111 | -2.062500 | -3/4 FS |
| -FS +1 LSB | -5.499916 | 0000 | 0000 0000 0001 | 1111 | 1111 1111 1110 | 1000 | 0000 0000 0001 | 0111 | 1111 1111 1110 | -2.749916 | -FS +1 LSB |
| -FS + 1/2 LSB | -5.499958 | LSB "0" to "1" | | LSB "1" to "0" | | LSB "0" to "1" | | LSB "1" to "0" | | -2.749958 | -FS + 1/2 LSB |
| -FS | -5.500000 | 0000 | 0000 0000 0000 | 1111 | 1111 1111 1111 | 1000 | 0000 0000 0000 | 0111 | 1111 1111 1111 | -2.750000 | -FS |
| | | OFFSET BINARY | | COMP. OFF. BIN. | | TWO'S COMP. | | COMP. TWO'S COMP. | | | |

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and -55 to +125°C. All room-temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically insulating, thermally-conductive "pads" may be installed

underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters," or contact DATEL directly, for additional information.

Scale is approximately 25ns per division. fs = 10MHz

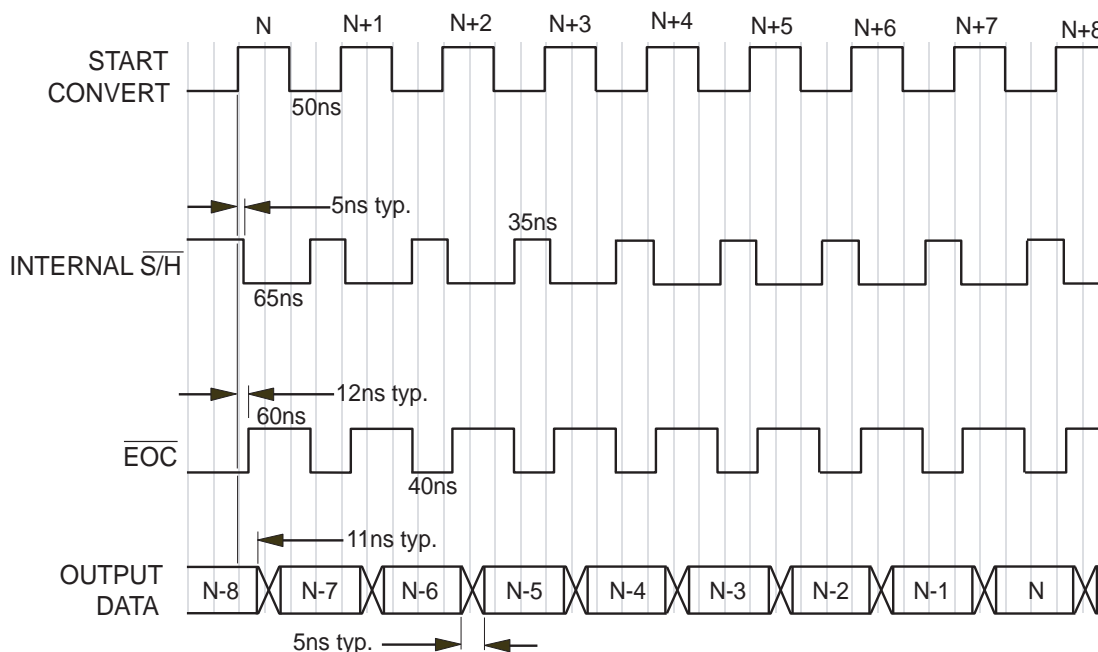
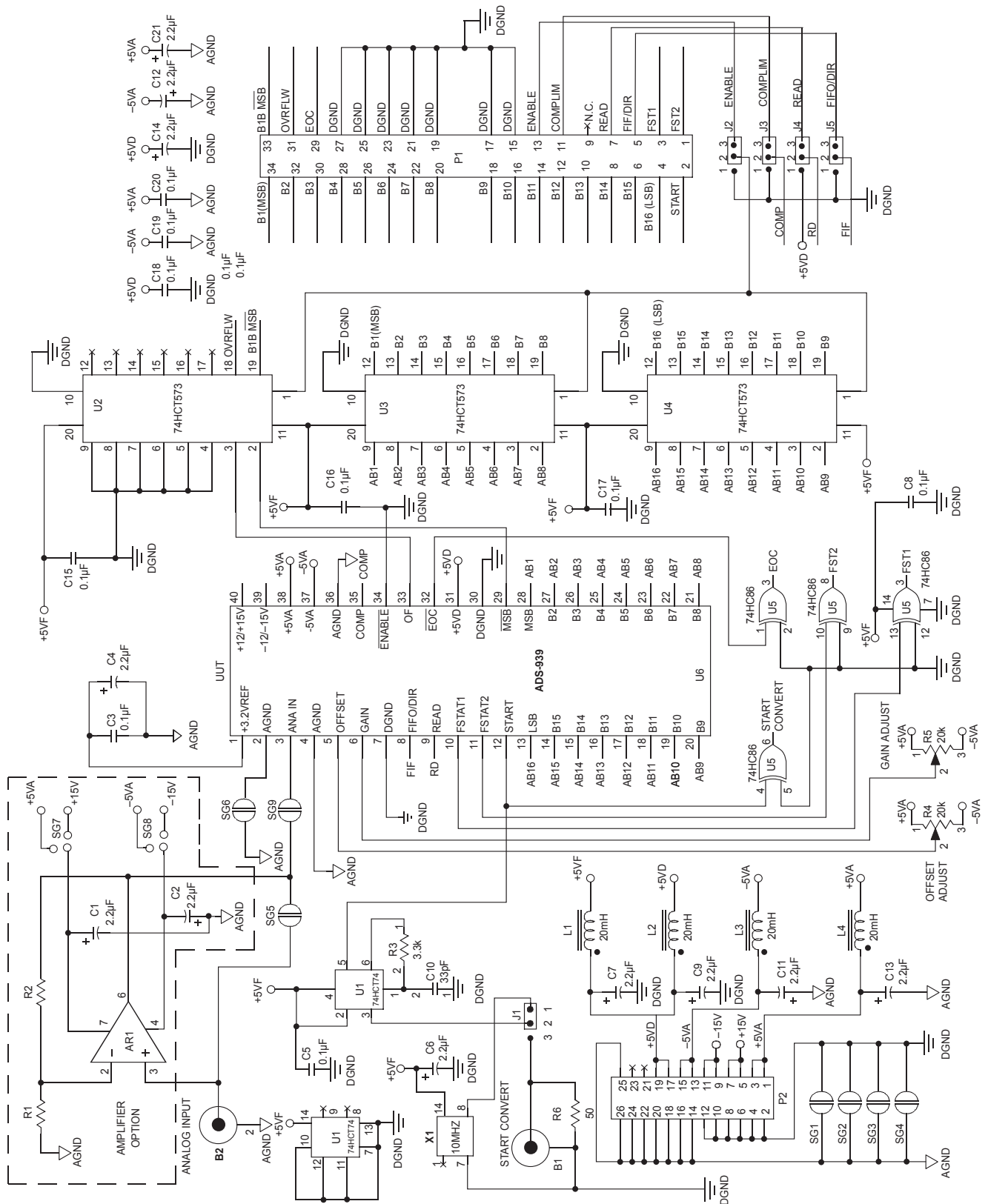


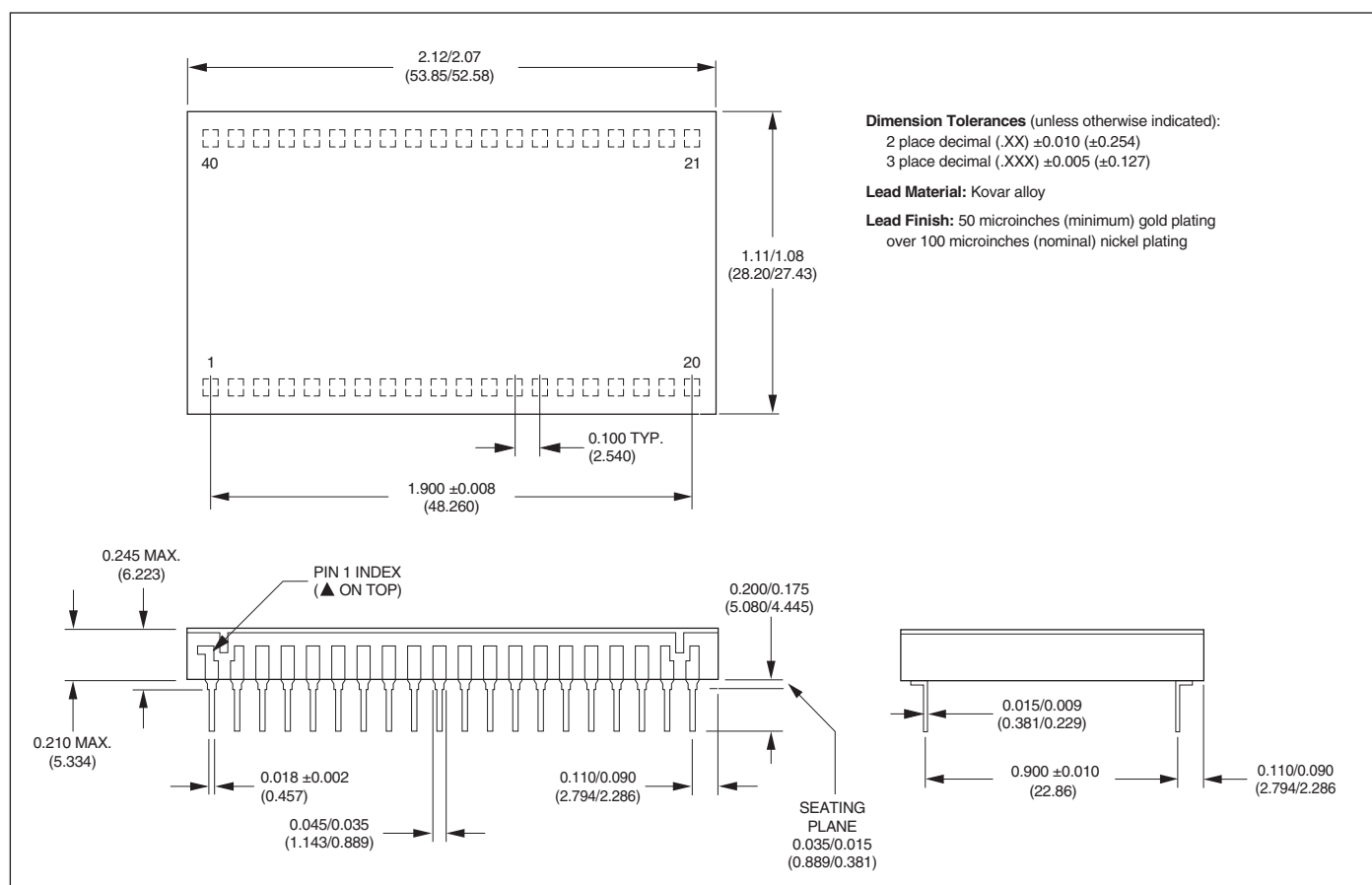
Figure 3. ADS-939 Timing Diagram



Preliminary Evaluation Board - Modified ADS-B933 to include $\pm 12V$ or $\pm 15V$ Supplies to U6

Figure 4. ADS-939 Evaluation Board Schematic.

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

| MODEL | OPERATING TEMP. RANGE | ACCESSORIES |
|-----------|-----------------------|---|
| ADS-939MC | 0 to +70°C | ADS-B939 Evaluation Board (without ADS-939) |
| ADS-939MM | -55 to +125°C | HS-40 Heat Sink for all ADS-939 models |

Receptacles for PC board mounting can be ordered through AMP, Inc., Part # 3-331272-8 (Component Lead Socket), 40 required. For MIL-STD-883 product, or surface mount packaging, contact DATEL.

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